

CP6001-V

**6U CompactPCI Processor Board based on
the Intel® Celeron® M 440 Processor with
the Intel® 945GM Express Chipset**

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User Guide



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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.



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High Voltage Safety Instructions



Warning!

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Caution, Electric Shock!

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Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.



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In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.



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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter

1

Introduction



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1. Introduction

1.1 Board Overview

The CP6001-V is a highly integrated 6U CompactPCI CPU board based on the Intel® Celeron® M 440 processor combined with the high-performance Mobile Intel® 945GM Express Chipset.

The board supports the Intel® Celeron® M processor 440 with 1.86 GHz clock speed, 533 MHz front-side bus speed as well as 64 kB L1 and 1 MB L2 cache provided in a 479 µFCBGA package, and utilizes the Mobile Intel® 945GM Express Chipset as Graphics Memory Controller Hub and the ICH7R as I/O Controller Hub.

Two SO-DIMM sockets are available on the board to provide up to 4 GB dual-channel, Double Data Rate (DDR2) memory running at 533 MHz (PC2-4200). The board also includes four Intel® 82574L Gigabit Ethernet controllers, each utilizing a x1 lane PCI Express interconnection to the ICH7R I/O Controller Hub. In addition, the board can accommodate a CompactFlash memory card and a USB 2.0 NAND Flash module for flexible, non-volatile, non-rotating memory extension. Onboard SATA HDD/SSD support is also provided via an optional CP6001-EXT-SATA module.

The CP6001-V offers a complete set of data and communication interfaces, such as four Gigabit Ethernet ports (two on front I/O and two on rear I/O), one Parallel ATA interface connected to the CompactFlash socket, two onboard Serial ATA interfaces (one for connecting a SATA cable and one for connecting a 2.5" HDD/SSD to the board), one high-resolution VGA interface (CRT), and one 32-bit/33 MHz PMC interface. In addition, three USB 2.0 ports are available on the board, two on the front panel, and one onboard port for the USB 2.0 NAND Flash module. One RS-232 COM port is also available on the front panel.

The board supports a configurable 32-bit, 33/66 MHz, hot swap CompactPCI interface. If installed in the system slot, the interface is enabled, and if installed in a peripheral slot, the CP6001-V is isolated from the CompactPCI bus.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments, including I/O intensive applications where only one slot is available for the CPU, making it a perfect core technology for long-life applications. Components with high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability.

The board is offered with Microsoft® Windows® XP, Windows® XP Embedded, and Linux operating systems. Please contact Kontron for further information concerning the operation of the CP6001-V with other operating systems.



1.2 Board-Specific Information

The CP6001-V is a CompactPCI single-board computer based on the Intel® Celeron® M processor 440 processor and specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP6001-V's outstanding features are:

- Intel® Celeron® M processor 440, 1.86 GHz, 533 MHz FSB, 1 MB L2 cache
- 479-pin µFCBGA package
- 64 kB L1 and up to 1 MB L2 cache on-die, running at CPU speed
- Mobile Intel® 945GM Express Chipset with Intel® 82801GR (ICH7R) I/O Controller Hub
- Up to 4 GB DDR2-SDRAM memory running at 533 MHz
- Integrated 3D high-performance VGA controller
- Analog display support for up to 2048 x 1536 pixels at 75 Hz
- 32-bit, 33/66 MHz CompactPCI interface (PICMG 2.0)
- PMC interface with bezel cutout on front panel and PCI functionality, 32-bit/33 MHz PCI
- Four Gigabit Ethernet interfaces utilizing a x1 lane PCI Express per GbE controller
 - Two Gigabit Ethernet interfaces on the front panel
 - Two optional Gigabit Ethernet interfaces on the rear I/O (PICMG 2.16)
- EIDE Ultra ATA interface for onboard CompactFlash socket (type I and type II CF cards)
- Two onboard Serial ATA interfaces
 - One standard Serial ATA interface for connecting a SATA cable
 - One Serial ATA interface for connecting a Serial ATA 2.5" HDD/SSD via the CP6001-EXT-SATA module
- Three USB 2.0 ports:
 - Two ports on the front panel
 - One onboard port for the USB 2.0 NAND Flash module
- One RS-232 COM port on the front panel
- One 1 MB soldered FWH for BIOS
- Hardware Monitor (Super I/O SCH3112)
- Watchdog Timer
- Real-time clock
- 4HP, 6U CompactPCI
- Passive heat sink solution for forced convection cooling
- Hot swap capability: as system controller or as peripheral device
- Supports PICMG Packet Switching Backplane Specification 2.16
- AMI BIOS



1.3 System Expansion Capabilities

1.3.1 PMC Module

The CP6001-V has one PCI, 32-bit/33 MHz PMC mezzanine interface. This interface supports a wide range of available PMC modules with PCI interface including all of Kontron's PMC modules and provides an easy and flexible way to configure the CP6001-V for various application requirements.

For further information concerning the PMC interface, refer to Chapter 2.3.8, PMC Interface.

1.3.2 CP6001-V-MK2.5SATA Assembly Kit

The CP6001-V comes with an optional CP6001-V-MK2.5SATA assembly kit comprised of one CP6001-EXT-SATA module and the necessary components needed for mounting the module on the CP6001-V. The CP6001-EXT-SATA module is required for connecting an onboard 2.5" Serial ATA HDD/SSD to the CP6001-V.

For further information concerning the CP6001-EXT-SATA module, refer to Appendix A.

1.3.3 USB 2.0 NAND Flash Module

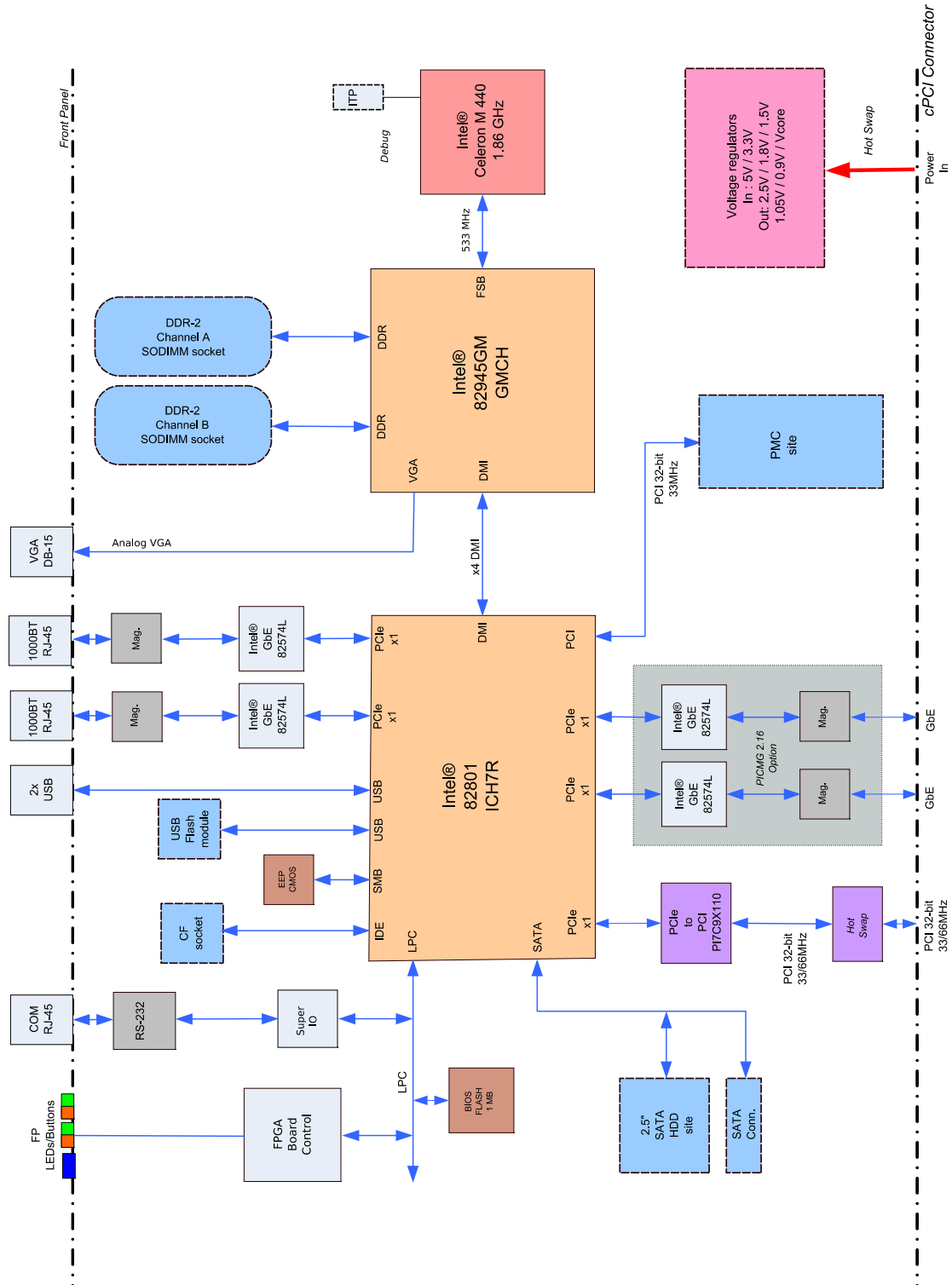
The CP6001-V provides support for one optional USB 2.0 NAND Flash module. For information on the USB 2.0 NAND Flash interface, refer to chapter 2.2.7.2, "USB 2.0 NAND Flash Module".

1.4 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.4.1 Functional Block Diagram

Figure 1-1: CP6001-V Functional Block Diagram





1.4.2 Front Panels

Figure 1-2: CP6001-V Front Panels

Legend:

Status LEDs

- WD (red/green): Watchdog Status
- TH (red/green/amber): Temperature Status
- HS (blue): Hot Swap Control

General Purpose LEDs

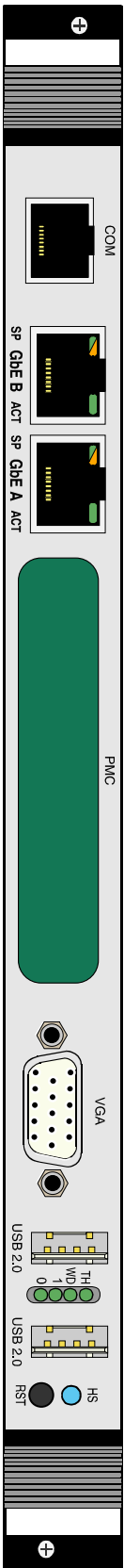
LED 0..1 (red/green/amber):General Purpose/POST code

Integral Ethernet LEDs

- ACT (green): Ethernet Link/Activity
- SPEED (green/orange): Ethernet Speed
- SPEED ON (orange): 1000 Mbit
- SPEED ON (green): 100 Mbit
- SPEED OFF: 10 Mbit



Note ...
If the General Purpose LEDs are lit red during boot-up, a failure is indicated before the BIOS has started.
For further information, please contact Kontron.



1.4.3 Board Layout

Figure 1-3: CP6001-V Board Layout (Front View)

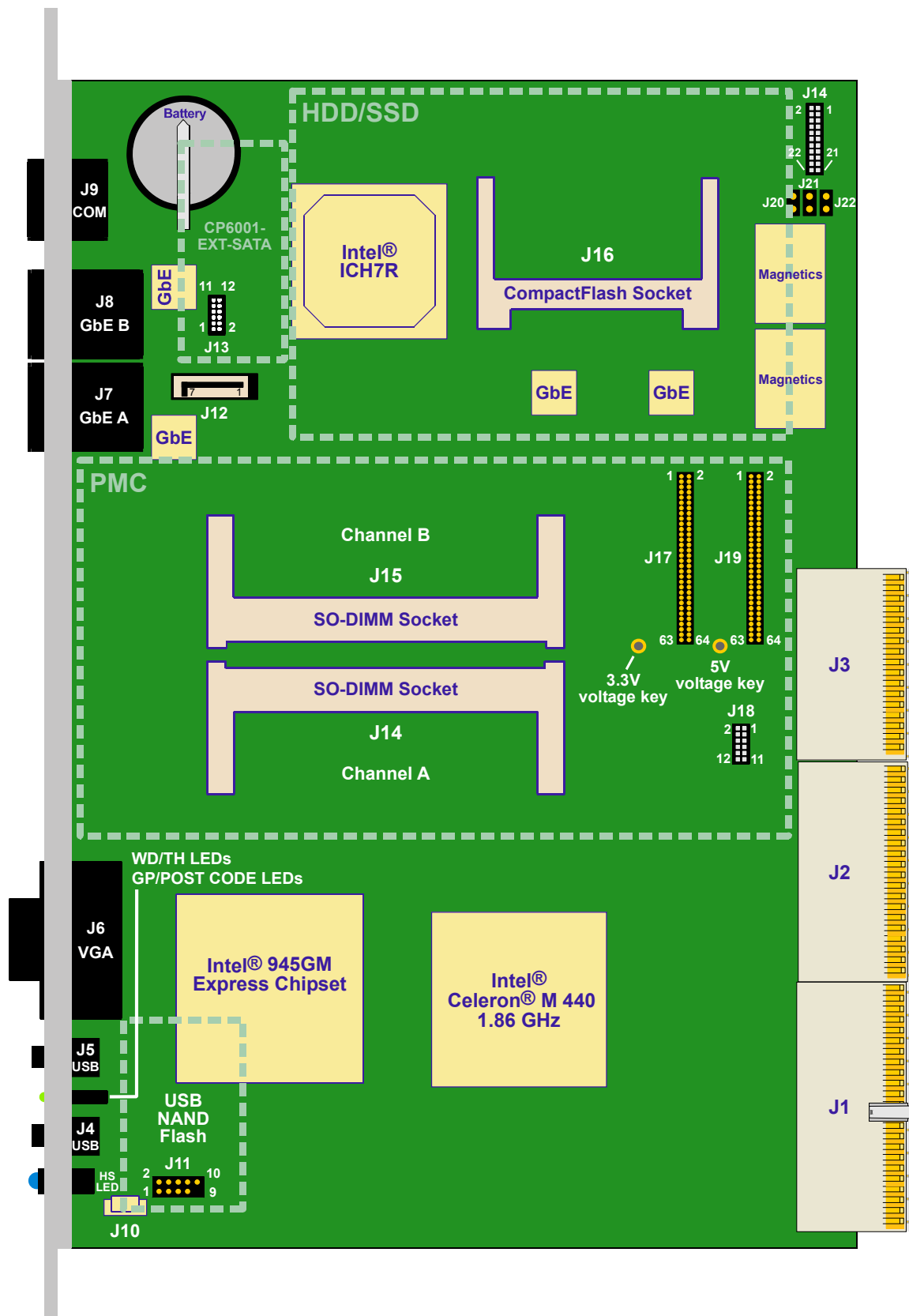
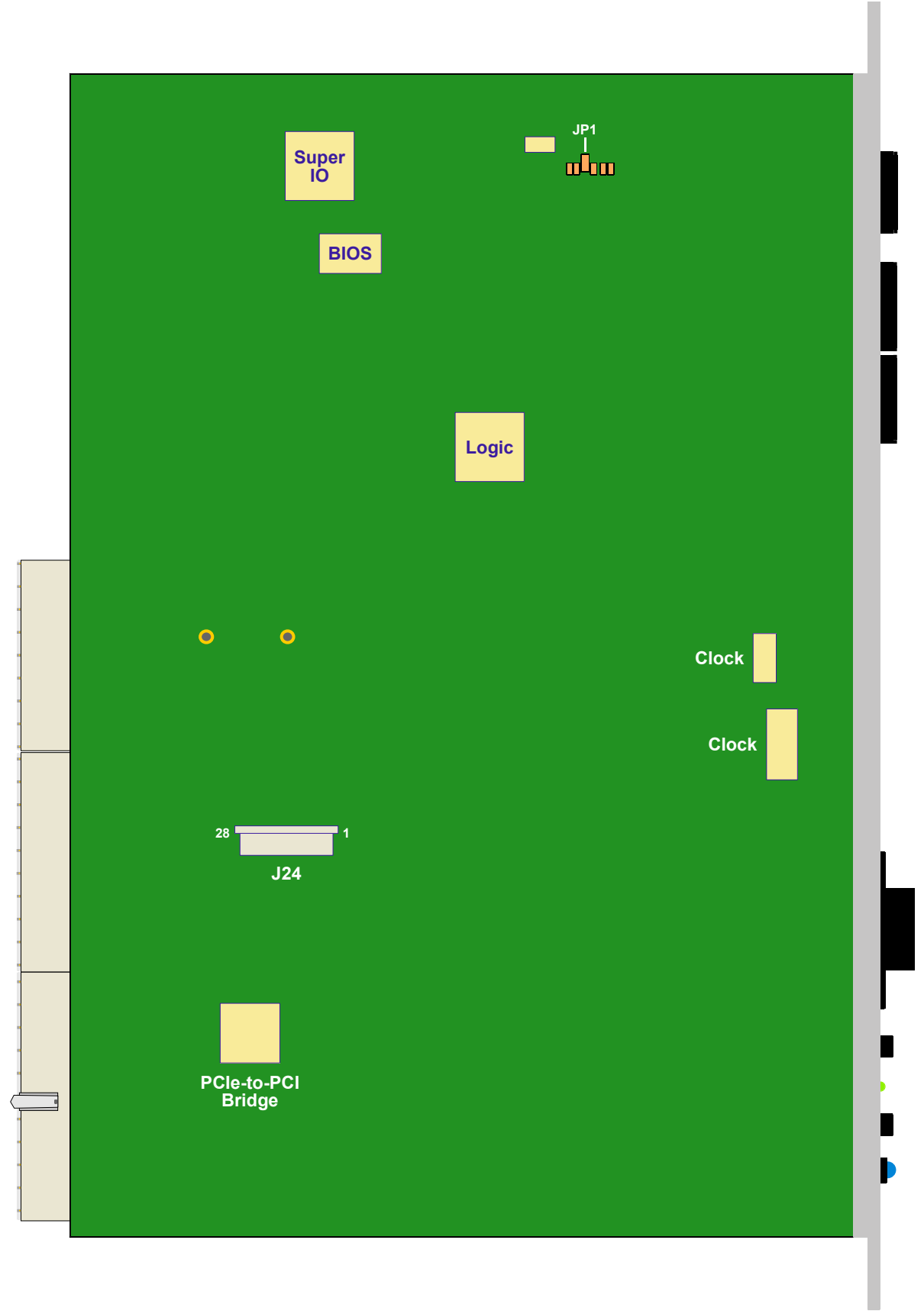


Figure 1-4: CP6001-V Board Layout (Reverse View)



1.5 Technical Specification

Table 1-1: CP6001-V Main Specifications

CP6001-V		SPECIFICATIONS
Processor and Memory	CPU	The CP6001-V supports the Intel® Celeron® M processor 440, 1.86 GHz, 533 MHz FSB, 1 MB L2 cache in a 479 µFCBGA packaging.
	Memory	<p>Main Memory:</p> <ul style="list-style-type: none"> Up to 4 GB dual-channel, DDR2 memory running at 533 MHz <p>Cache structure:</p> <ul style="list-style-type: none"> 64 kB L1 on-die full speed processor cache <ul style="list-style-type: none"> 32 kB for instruction cache 32 kB for data cache 1 MB L2 on-die full speed processor cache <p>FLASH Memory:</p> <ul style="list-style-type: none"> One 1 MB onboard FWH for BIOS CompactFlash memory optionally available USB 2.0 NAND Flash memory optionally available (e.g. 8 GB) Serial ATA SSD Flash memory optionally available <p>Serial EEPROM:</p> <ul style="list-style-type: none"> 24LC64 (64 kbit)
Chipset	Intel® 945GM Express GMCH	<p>Mobile Intel® 945GM Express Graphics Memory Controller Hub:</p> <ul style="list-style-type: none"> Support for a single Intel® Celeron® M processor 440 64-bit AGTL/AGTL+ based System Bus interface up to 533 MHz System Memory interface with optimized support for dual-channel DDR2 SDRAM memory at 533 MHz without ECC Integrated 2D and 3D Graphics Engines Integrated 400 MHz RAMDAC
	Intel® ICH7R	<p>Intel® 82801GR I/O Controller Hub (ICH7R):</p> <ul style="list-style-type: none"> Power management logic support Enhanced DMA controller, interrupt controller, and timer functions Integrated IDE controller Ultra ATA/100/66/33 and PIO mode USB 2.0 host interface with seven USB ports (only three ports are used on the CP6001-V) SATA Host Controller with two ports, 3 Gbit/s transfer rate Five of the six x1 PCI Express ports are used on the CP6001-V: <ul style="list-style-type: none"> Four x1 PCI Express ports are used for Gigabit Ethernet One x1 PCI Express port is used for the PCIe-to-CPCI bridge System Management Bus (SMBus) compatible with most I²C™ devices Low Pin Count (LPC) interface Firmware Hub (FWH) interface support



Table 1-1: CP6001-V Main Specifications (Continued)

CP6001-V		SPECIFICATIONS
Interfaces	CompactPCI	<p>Compliant with the CompactPCI Specification PICMG 2.0 R3.0:</p> <ul style="list-style-type: none"> • System controller operation • 32-bit, 33/66 MHz PCI master interface • 3.3V or 5V signaling levels (universal signaling support) <p>Compliant with Packet Switching Specification PICMG 2.16 R1.0</p> <p>When installed in a peripheral slot, the CP6001-V is electrically isolated from the CompactPCI bus. It receives power from the backplane and supports rear I/O in compliance with the PICMG 2.16 specification.</p>
	Rear I/O	<p>The following interfaces are routed to the rear I/O connector J3:</p> <ul style="list-style-type: none"> • 2 x Gigabit Ethernet (compliant with PICMG 2.16)
	Hot Swap Compatible	<p>The CP6001-V supports System Master hot swap functionality and application dependent hot swap functionality when used in a peripheral slot.</p> <p>When used as a System Master, the CP6001-V supports individual clocks for each slot and the ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification.</p>
	VGA	<p>Built-in Intel 3D Graphics accelerator for enhanced graphics performance.</p> <ul style="list-style-type: none"> • Supports resolutions of up to 2048 x 1536 at a 75 Hz refresh rate • Hardware motion compensation for software MPEG2 decoding • Dynamic Video Memory Technology (DVMT3.0)
	Gigabit Ethernet	<p>Up to four 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on the Intel® 82574L Ethernet PCI Express bus controllers:</p> <ul style="list-style-type: none"> • Two RJ-45 connectors on front panel • Two optional Gigabit Ethernet interfaces on the rear I/O connector J3 (PICMG 2.16) • Automatic mode recognition (Auto-Negotiation) • Automatic cabling configuration recognition (Auto MDI-X) <p>Cabling requirement: Category 5, UTP, four-pair cabling</p>
	USB	<p>Three USB 2.0 ports supporting UHCI and EHCI:</p> <ul style="list-style-type: none"> • Two type A connectors on the front panel • One onboard connector for the USB 2.0 NAND Flash module

Table 1-1: CP6001-V Main Specifications (Continued)

CP6001-V		SPECIFICATIONS
Interfaces	Serial	One 16C550-compatible UART on the front panel (RS-232 signaling)
	PMC	PMC interface: <ul style="list-style-type: none"> • Jn1 and Jn2 PCI mezzanine connectors for standard PMC modules • 32-bit/33 MHz PCI interface • Supported voltages: 3.3 V, 5 V, +12 V, and -12 V • Supports 3.3 V / 5V signaling voltage (V/I/O)
	Keyboard and Mouse	USB Support for keyboard and mouse
	Mass Storage	EIDE ATA: <ul style="list-style-type: none"> • One onboard ATA interface for the CompactFlash socket supporting type I and type II CompactFlash cards (true IDE mode and Multiword DMA support) SATA: Integrated Serial ATA Host Controllers <ul style="list-style-type: none"> • Provide independent DMA operation on 2 channels: <ul style="list-style-type: none"> • One onboard SATA interface for connection to a SATA cable • One onboard SATA interface for connection to the CP6001-EXT-SATA module Onboard 2.5" HDD/SSD: <ul style="list-style-type: none"> • Onboard 2.5" Hard Disk Drive (HDD) or Solid State Drive (SSD) is supported via the 12-pin Serial ATA connector, J13, and the CP6001-EXT-SATA module
Sockets	Front Panel Connectors	<ul style="list-style-type: none"> • VGA: 15-pin, D-Sub connector • USB: two type A connectors • Ethernet: two RJ-45 connectors • COM: 8-pin, RJ-45 connector • PMC front panel
	Onboard Connectors	Onboard connectors: <ul style="list-style-type: none"> • USB 2.0 NAND Flash connector, J11 • I/O extension connector, J14 • PMC connectors J17 and J19 (Jn1 and Jn2) • Two SATA connectors: <ul style="list-style-type: none"> • One 7-pin, standard SATA connector with locking mechanism, J12 • One 12-pin, SATA extension connector, J13 • CompactPCI Connector J1 to J3 • One CompactFlash socket for type I and type II CF cards, J16 • One JTAG connector, J18 • One ITP700 JTAG connector, J24 • Two 200-pin SO-DIMM sockets, J14 and J15





Table 1-1: CP6001-V Main Specifications (Continued)

CP6001-V		SPECIFICATIONS
HW Monitoring	LEDs	<p>System Status LEDs:</p> <ul style="list-style-type: none"> WD (red/green): Watchdog Status TH (red/green/amber): Temperature Status HS (blue): Hot Swap Control <p>General Purpose LEDs:</p> <ul style="list-style-type: none"> LED 0..1 (red/green/amber): General Purpose/POST code <p>Gigabit Ethernet Status:</p> <ul style="list-style-type: none"> ACT (green): Ethernet Link/Activity SPEED (green/orange): Ethernet Speed SPEED ON (orange): 1000 Mbit SPEED ON (green): 100 Mbit SPEED OFF: 10 Mbit
	Watchdog	Software configurable Watchdog generates IRQ or hardware reset.
	Thermal-Related Functions	<p>CPU overtemperature protection is provided by:</p> <ul style="list-style-type: none"> Internal processor temperature control unit CPU shut down via the hardware monitor
	System Monitoring	<p>In SCH3112 integrated hardware monitor for supervision of:</p> <ul style="list-style-type: none"> Several system power voltages Board temperature
Software	Software BIOS	<p>AMI BIOS with 1 MB Flash memory and the following features:</p> <ul style="list-style-type: none"> User BIOS defaults (Setup Default Override - SDO) ACPI support FWH write protection (BIOS Flash) Fail-safe mechanism <ul style="list-style-type: none"> Boot block recovery CMOS parameters are saved in the EEPROM PC Health Monitoring Manufacturing data: <ul style="list-style-type: none"> Serial number Material number Chipset revision CPU microcode
	Operating Systems	<p>Operating systems supported:</p> <ul style="list-style-type: none"> Microsoft® Windows® XP Microsoft® Windows® XP Embedded Linux



Table 1-1: CP6001-V Main Specifications (Continued)

CP6001-V		SPECIFICATIONS
General	Mechanical	6U, 4HP, CompactPCI-compliant form factor
	Power Consumption	Typical 24 W Refer to Chapter 5 for further information.
	Temperature Ranges	Operational: 0°C to +60°C Standard Storage: -55°C to +85°C Without battery or any additional components  Note ... When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP6001-V (See "Battery" below).  Note ... When additional components are installed, refer to their operational specifications as this will influence the operational and storage temperature of the CP6001-V.
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 160 mm
	Board Weight	550 g 4HP with heat sink and SO-DIMM modules but without mezzanine boards such as PMC module, HDD/SSD, and CP6001-EXT-SATA module
	Battery	The CP6001-V provides a 3.0V lithium battery for RTC with battery socket. Recommended type: CR2025 Temperature ranges: Operational: -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage: -55°C to +70°C typical (no discharge)

1.6 Kontron Software Support

Kontron is one of the few CompactPCI and VME manufacturers providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.



1.7 Standards

The CP6001-V complies with the requirements of the following standards:

Table 1-2: Standards

TYPE	ASPECT	STANDARD
CE	Emission	EN55022 EN61000-6-3
	Immission	EN55024 EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE 1101.10
Environmental	Climatic Humidity	IEC60068-2-78
	WEEE	Directive 2002/96/EC Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC Restriction of the use of certain hazardous substances in electrical and electronic equipment

1.8 Related Publications

The following publications contain information relating to this product.

Table 1-3: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification PICMG 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 1.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	<i>Kontron</i> CompactPCI Backplane Manual, ID 24229
CompactFlash Cards	CF+ and CompactFlash Specification Revision 2.1
PMC Modules	IEEE 1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family IEEE 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142



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Chapter

2

Functional Description



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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The CP6001-V supports the latest Intel® Celeron® M 440 processor with 1.86 GHz processor speed and 533 MHz FSB. The following list sets out some of the key features of this processor:

- Supports Intel Architecture with Dynamic Execution
- On-die, primary 32 kB instruction cache and 32 kB write-back data cache
- On-die, 1MB second level cache with Advanced Transfer Cache Architecture
- Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- Streaming SIMD Extensions 3 (SSE3)
- 533 MHz Front Side Bus (FSB)
- Digital Thermal Sensor
- Execute Disable Bit support for enhanced security

The following tables provide information about the Intel® Celeron® M 440 processor supported on the CP6001-V including its maximum power dissipation.

Table 2-1: Intel® Celeron® M 440 Processor Supported on the CP6001-V

SPEED	Intel® Celeron® M 440 1.86 GHz
PACKAGE	µFCBGA
L2 CACHE	1 MB
FSB	533 MHz
MAX. POWER	27 W



2.1.2 Memory

The CP6001-V supports a dual-channel DDR2 memory without Error Checking and Correcting (ECC) running at 533 MHz (PC2-4200). The maximum memory size per channel is 2 GB. The available memory configuration can be either 512 MB, 1 GB, 2 GB, or 4 GB. The maximum address space for the entire board is 4 GB and is limited by the chipset. For this reason, there is less than 4 GB physical memory available for applications. The integrated VGA controller uses up to 128 MB physical memory as well.

**Note ...**

Only qualified DDR2 SO-DIMM modules from Kontron are authorized for use with the CP6001-V.

Table 2-2: Supported/Recommended Memory Configurations

CHANNEL A (SO-DIMM)	Channel B (SO-DIMM)	TOTAL
512 MB	--	512 MB
512 MB	512 MB	1 GB
1 GB	--	1 GB
1 GB	1 GB	2 GB
2 GB	--	2 GB
2 GB	2 GB	4 GB

**Warning!**

Memory configuration changes are only permitted to be performed at the factory.

Failure to comply with the above may result in damage to the board or improper operation.

2.1.3 Intel® 945GM Express Chipset Overview

The Intel® 945GM Express Chipset consists of the following devices:

- Mobile Intel® 945GM Express Chipset Graphics Memory Controller Hub (945GM Express Chipset GMCH)
- I/O Controller Hub 7 (ICH7R)

The 945GM Express Chipset GMCH provides the processor interface for the Intel® Celeron® M 440 processor and the two DDR2 channels, and includes a high-performance graphics accelerator. The ICH7R is a centralized controller for the boards' I/O peripherals, such as the PCI, PCI Express, USB 2.0, SATA II, IDE and LPC ports.

2.1.4 Mobile Intel® 945GM Express Chipset GMCH

The Mobile Intel® 945GM Express Chipset Graphics Memory Controller Hub (945GM Express Chipset GMCH) is a highly integrated hub that provides the CPU interface, two DDR2 SDRAM system memory interfaces at 533 MHz, a hub link interface to the ICH7R and high-performance internal graphics controller.



Graphics and Memory Controller Hub Feature Set

Host Interface

The 945GM Express Chipset GMCH supports a Front Side Bus (FSB) frequency of 533 MHz using 1.05 V AGTL signaling. The AGTL bus supports 32-bit host addressing for decoding up to 4 GB memory address space.

System Memory Interface

The 945GM Express Chipset GMCH integrates a dual-channel DDR2 SDRAM controller with two 64-bit interfaces without ECC bits. The chipset supports DDR533 DDR2 SDRAM for system memory.

945GM Express Chipset GMCH

The 945GM Express Chipset GMCH includes a highly integrated graphics accelerator delivering high-performance 3D and 2D graphic capabilities. The internal graphics controller provides an interface for a standard analog VGA display.

2.1.5 I/O Controller Hub (ICH7R)

The ICH7R is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms, for example, PCI Express, Ultra DMA 100/66/33 IDE controller, SATA controller, USB host controller supporting USB 2.0, LPC interface, and a FWH Flash BIOS interface controller. The ICH7R communicates with the 945GM Express Chipset GMCH over a dedicated hub interface.

I/O Controller Hub Feature set comprises:

- PCI 2.3 interface with eight PCI IRQ inputs
- Bus master IDE controller UltraDMA 100/66/33 or PIO mode
- Five USB controllers with up to eight USB 1.1 or USB 2.0 ports (max. of 3 ports used on the CP6001-V)
- Hub interface for a 945GM Express Chipset
- FWH interface
- LPC interface
- RTC controller

2.2 Peripherals

The following standard peripherals are available on the CP6001-V board:

2.2.1 Timer

The CP6001-V is equipped with the following timers:

- Real-time clock (RTC)
The ICH7R contains an MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM.
The real-time clock performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. All CMOS RAM data from the RTC remains stored in an additional EEPROM. This prevents data loss in case the CP6001-V is operated without battery.
- Hardware delay timer for short reliable delay times



2.2.2 Watchdog Timer

A Watchdog Timer is provided, which forces either an IRQ5, or a reset condition (configurable in the Watchdog Register). The Watchdog Timer can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the Watchdog Timer is enabled, it cannot be stopped.

2.2.3 Reset

The CP6001-V is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.7 V for the 5 V line and below 3.1 V for the 3.3 V line, or in the event of a power failure of the DC/DC converters. Other reset sources include the Watchdog Timer and the push-button switch on the front panel. The CP6001-V responds to any of these sources by initializing local peripherals.

A reset will be generated if one of the following events occurs:

- +5 V supply falls below 4.7 V (typ.)
- +3.3 V supply falls below 3.1 V (typ.)
- Power failure of at least one onboard DC/DC converter
- Push-button "RESET" pressed (on the front panel)
- Watchdog expired
- CompactPCI backplane PRST input
- CompactPCI backplane RST input (software-configurable when the board is in peripheral mode)

2.2.4 SMBus Devices

The CP6001-V provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I²C bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-3: SMBus Device Addresses

DEVICE	SMB ADDRESS
EEPROM 24LC64	1010111xb
Clock (core)	1101001xb
Clock (PCI Express)	1101110xb
SPD (channel A)	1010000xb
SPD (channel B)	1010010xb

2.2.5 Thermal Management/System Monitoring

The SCH3112 is used to measure the ambient temperature via its own internal sensor and monitors the CPU's internal temperature to ensure proper operation and stability of the system.



2.2.6 Serial EEPROM

This EEPROM is connected to the SMBus provided by ICH7R.

Table 2-4: EEPROM Address Map

ADDRESS	FUNCTION
0x000 - 0x0FF	CMOS backup
0x100 - 0x1FF	Production data
0x200 - 0x3FF	OS Boot parameter
0x400 - 0x1FFF	User

2.2.7 FLASH Memory

There are up to four Flash devices available as described below, one for the BIOS and three for data storage.

2.2.7.1 BIOS FLASH (Firmware Hub)

The CP6001-V provides one 1 MB Firmware Hub Flash chip for the BIOS.

2.2.7.2 USB 2.0 NAND Flash Module

The CP6001-V supports one optional USB 2.0 NAND Flash module qualified by Kontron. The USB 2.0 NAND Flash module is connected to the onboard connector J11.

The USB 2.0 NAND Flash module is a USB 2.0 based NAND Flash drive with a built-in full hard-disk emulation and a high data transfer rate. It is optimized for embedded systems providing high-performance, reliability and security.

2.2.7.3 CompactFlash Socket

To enable flexible Flash extension, an onboard CompactFlash (CF) type II socket, J16, is available underneath the HDD module.

CompactFlash is a very small removable mass storage device. It provides true IDE functionality compatible with the 16-bit ATA/ATAPI-4 interface.

The CompactFlash socket is connected to the IDE port of the ICH7R and is set to master configuration.

The CP6001-V supports DMA as well as both CF type I and CF type II.



2.3 Board Interfaces

2.3.1 Front Panel LEDs

The CP6001-V is equipped with one Watchdog Status LED (WD LED), one Temperature Status LED (TH LED), two General Purpose/POST code LEDs (LED0..1), and one Hot Swap LED (HS LED). Their functionality is described in the following chapters and reflected in the registers mentioned in Chapter 4, Configuration.

2.3.1.1 Hot Swap LED

On the CP6001-V, a blue HS LED is provided, for example, to indicate the status of the shut-down process and when the board is ready for extraction.

Table 2-5: Hot Swap LED Function

LED	COLOR	NORMAL MODE	OVERRIDE MODE
HS LED	blue	On = ready for hot swap (board may be extracted) Off = board in normal operation (do not extract the board) Blinking = change of status to On/Off	Selectable by user: • Only lamp test

2.3.1.2 Watchdog and Temperature Status LEDs

The CP6001-V provides one LED for the Watchdog Status (WD LED) and one for the Temperature Status (TH LED).



Note ...

If the TH LED is lit amber, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. Once activated, Thermtrip remains latched until a cold restart of the CP6001-V is undertaken (all power off and then on again).

Table 2-6: Watchdog and Temperature Status LEDs Function

LED	COLOR	FUNCTION DURING BIOS POST	FUNCTION AFTER BOOT-UP (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP (if POST code config. is disabled)
WD LED	red	--	--	Watchdog expired
	green	BIOS POST bit 1 and bit 5	BIOS POST bit 1 and bit 5	Watchdog active, waiting to be triggered
TH LED	off	--	--	The TH LED is off if the CPU temperature is below 100°C (normal operation).
	red	--	--	The TH LED blinks red if the CPU temperature is above 100°C but below 125 °C.
	green	BIOS POST bit 0 and bit 4	BIOS POST bit 0 and bit 4	--
	amber	--	--	If the CPU has been shut off, i.e. the CPU has reached a temperature above 125°C. In this event, the TH LED remains lit.



2.3.1.3 General Purpose LEDs

The CP6001-V provides two General Purpose LEDs (LED0..1) on the front panel. They are designed to indicate the boot-up POST code after which they are available to the application.

If the LED0..1 are lit red during boot-up, a failure is indicated before the BIOS has started. In this case, check the power supply. If the power supply appears to be functional and the LEDs are still red, please contact Kontron for further assistance.

The POST code is indicated during the boot-up phase. After boot-up, the LEDs indicate General Purpose or Port 80 signals, depending on the BIOS settings. The default setting after boot-up is General Purpose.

Table 2-7: General Purpose LEDs Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING BIOS POST (if POST code config. is enabled)	DEFAULT FUNCTION AFTER BOOT-UP
LED1	red	When lit up during boot-up, it indicates a hardware reset.	--	General Purpose or Port 80 Default: General Purpose
	green	--	BIOS POST bit 2 and bit 6	
	amber	--	--	
LED0	red	When lit up during boot-up, it indicates a power-on reset.	--	General Purpose or Port 80 Default: General Purpose
	green	--	BIOS POST bit 3 and bit 7	
	amber	--	--	

For further information on configuring the General Purpose LEDs, refer to Chapter 4.3.12, "LED Configuration Register (LCFG)", and Chapter 4.3.13, "LED Control Register (LCTRL)".



2.3.2 How to Read the 8-Bit POST Code

Due to the fact that only 4 bits are available and 8 bits must be displayed, the POST code output is multiplexed on the WD LED, TH LED and the General Purpose LEDs.

Table 2-8: POST Code Sequence

STATE	GENERAL PURPOSE LEDs
0	All LEDs are OFF; start of sequence
1	High nibble
2	Low nibble

The following is an example of the operation of the Temperature Status LED, Watchdog Status LED and General Purpose LEDs if POST configuration is enabled (see also Table 2-6, "Watchdog and Temperature Status LEDs Function" and Table 2-7, "General Purpose LEDs Function").

Table 2-9: POST Code Example

	LED0	LED1	WD	TH	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
POST CODE					0x41



Note ...

Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CP6001-V does not boot, please contact the Kontron for further assistance.



2.3.3 USB Interfaces

The CP6001-V supports three USB 2.0 ports (two on the front I/O and one onboard for the USB 2.0 NAND Flash module). All three ports are high-speed, full-speed, and low-speed capable. High-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

One USB peripheral may be connected to each port. For connecting more USB devices to the CP6001-V than there are available ports, an external USB hub is required.



Note ...

The USB host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.3.3.1 Front Panel USB Connectors J4 and J5

The CP6001-V has two USB 2.0 interfaces implemented as two, 4-pin, type A USB connectors on the front panel, J4 and J5, with the following pinout:

Figure 2-1: USB Con. J4 and J5

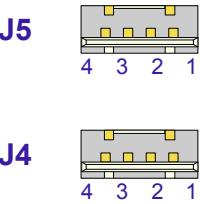


Table 2-10: USB Con. J4 and J5 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--



Note ...

Windows kernel debugging is supported via the USB Port 0 of the ICH7R chipset. The USB Port 0 is routed to the USB connector J5.



2.3.3.2 Onboard USB NAND Flash Connector J19

The CP6001-V has one onboard USB 2.0 interface for connecting an optional USB 2.0 NAND Flash mezzanine module. This interface is implemented as a 10-pin connector, J19, with the following pinout.

Figure 2-2: USB NAND Flash Con. J19 **Table 2-11: USB NAND Flash Con. J19 Pinout**



PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
3	UV0-	Differential USB-	I/O
5	UV0+	Differential USB+	I/O
7	GND	GND	--
9	Key		
2, 4, 6, 8	NC	Not connected	--
10	Res.	Reserved	--

2.3.4 Graphics Controller

The 945GM Express GMCH includes a highly integrated graphics accelerator delivering high-performance 3D, 2D graphics capabilities.

Integrated 2D/3D Graphics:

- Intel® Gen3.5 integrated graphics engine
- Smart 2D display technology (S2DDT)
- Dynamic video memory technology
- Integrated 400 MHz RAMDAC
- Resolution up to 2048 x 1536 pixels @ 75 Hz (QXGA)
- Integrated H/W Motion Compensation for MPEG2 decode

Graphics Memory Usage

The 945GM Express GMCH supports the Dynamic Video Memory Technology (DVMT 3.0). This technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

The graphics controller is fed with data from the 945GM Express GMCH. The graphics performance is directly related to the amount of memory bandwidth available.

Graphics Resolution

The 945GM Express GMCH has an integrated 400 MHz RAMDAC that can directly drive a progressive scan analog monitor up to a resolution of 2048 x 1536 pixels @ 75 Hz.

Graphics Interfaces

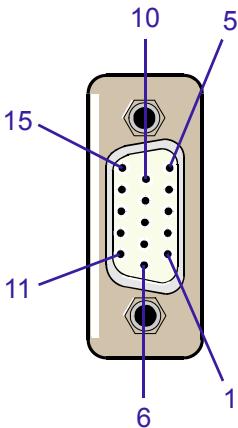
The internal graphics controller provides one analog VGA interface on the front panel.



Analog VGA Connector J6

The 15-pin female connector, J6, is available on the CP6001-V and is used to connect an analog VGA monitor to the CP6001-V.

Figure 2-3: D-Sub VGA Con. J6 Table 2-12: D-Sub VGA Connector J6 Pinout



PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
10	GND	Ground signal	--
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I ² C data (EDID)	I/O
15	Sclk	I ² C clock (EDID)	I/O
9	VCC	Power +5V, 1.5 A fuse protection	O
5,6,7,8	GND	Ground signal	--
4,11	NC	--	--

2.3.5 COM Port

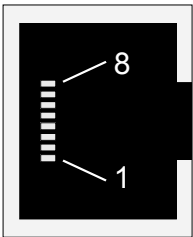
The CP6001-V provides one RS-232 COM port (COM1) implemented as an RJ-45 connector on the front panel.

COM1 is fully compatible with the 16550 controller, includes a sub-set of handshaking and modem control signals and provides maskable interrupt generation. The data transfer on the COM port is up to 115.2 kbit/s.

The following figure and table provide pinout information for the serial connector J9 (COM1).

Figure 2-4: Serial Con. J9 (COM1)

Table 2-13: Serial Con. J9 (COM1) Pinout



PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data set ready	I
8	CTS	Clear to send	I



2.3.6 Gigabit Ethernet

The CP6001-V provides four 10Base-T/100Base-TX/1000Base-T Gigabit Ethernet interfaces, two on the front panel (GbE A and GbE B) and two on the rear I/O (GbE C and GbE D) in accordance with the PICMG 2.16 specification.

The Gigabit Ethernet interfaces on the CP6001-V are based on the Intel® 82574L Gigabit Ethernet controllers, which are connected to the PCI Express interface. The Intel® 82574L Gigabit Ethernet Controller's architecture is optimized to deliver high-performance with the lowest power consumption. The controller's architecture includes independent transmit and receive queues and a PCI Express interface that maximizes the use of bursts for efficient bus usage. The Boot from LAN (PXE) feature is supported.

The Ethernet connectors J7 and J8 are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto MDI-X).

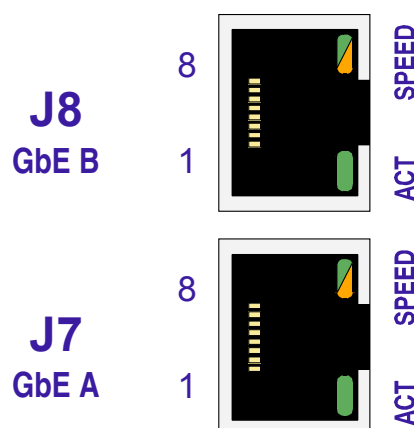
RJ-45 Connectors J7 and J8 Pinout

The J7 and J8 connectors supply the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table 2-14: Pinout of J7 and J8 Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDI-X / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Figure 2-5: Gigabit Ethernet Connectors J7 and J8





Ethernet LED Status

ACT (green): This LED indicates network connection and activity status. When this LED is lit, it means that a link has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED is not lit, there is no link established.

SPEED (green/orange): This LED lights up to indicate a successful 100Base-TX or 1000Base-T connection. When green, it indicates a 100Base-TX connection, and when orange, it indicates a 1000Base-TX connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.

2.3.7 Serial ATA Interface

The CP6001-V provides two Serial ATA (SATA) interfaces implemented as onboard SATA connectors. The SATA interfaces support SATA I (1.5 Gbit/sec) and SATA II (3.0 Gbit/sec). One of the onboard SATA connectors supports the mounting of an onboard 2.5" HDD/SSD. The other SATA connector is used for standard SATA devices with cable connection.

All SATA interfaces are realized as SATA II with a data transmission of up to 300 MB/s and are compatible with SATA I.

2.3.7.1 Serial ATA Connector J12

The CP6001-V provides a SATA connector, J12, for connecting standard HDDs/SSDs and other SATA devices to the CP6001-V.

Figure 2-6: SATA Con. J12



Table 2-15: SATA Connector J12 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground signal	--
2	SATA_TX0+	Differential Transmit +	O
3	SATA_TX0-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX0-	Differential Receive -	I
6	SATA_RX0+	Differential Receive +	I
7	GND	Ground signal	--



Note ...

If the onboard SATA connector, J12, will be used, due to the big SATA connector and the stiff SATA cable, the CP6001-V will exceed the thickness of 4HP.



Note ...

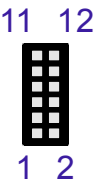
To ensure secure connectivity, the SATA connector supports the use of SATA II cables (SATA cables with locking latch).



2.3.7.2 2.5" SATA HDD/SSD Extension Connectors J13

The CP6001-V provides one 12-pin, female SATA extension connector, J13, for connecting an onboard 2.5" Serial ATA HDD/SSD to the CP6001-V through the CP6001-EXT-SATA module. For further information concerning the CP6001-EXT-SATA module, refer to Appendix A.

Figure 2-7: SATA Ext. Con. J13 Table 2-16: SATA Extension Connector J13 Pinout



PIN	SIGNAL	FUNCTION	I/O
1	SATA_RX2-	Differential Receive -	I
2	GND	Ground signal	--
3	SATA_RX2+	Differential Receive +	I
4	GND	Ground signal	--
5	GND	Ground signal	--
6	5V	5V power	--
7	SATA_TX2-	Differential Transmit -	O
8	GND	Ground signal	--
9	SATA_TX2+	Differential Transmit +	O
10	GND	Ground signal	--
11	GND	Ground signal	--
12	5V	5V power	--

2.3.8 PMC Interface

The CP6001-V allows installing a PMC module on the board. For flexible and easy configuration two PMC connectors, J17 and J19, are available. The J17 (Jn1) and J19 (Jn2) connectors provide the signals for the 32-bit PCI Bus.

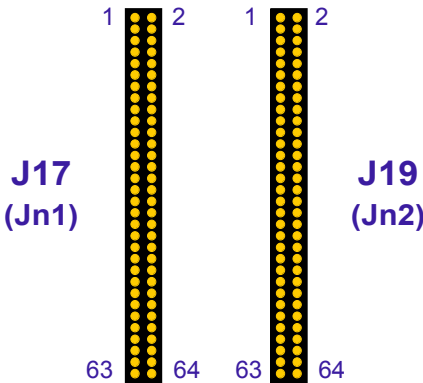
This interface has been designed to comply with the IEEE1386.1 specification, which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP6001-V provides 3.3V PMC PCI signaling environment. If 5V PMC PCI signaling environment is required, please contact Kontron for further assistance.

The PMC interface supports the following configuration:

Table 2-17: Onboard PCI Configuration

SIZE	SPEED	INTERFACE
32-bit	33 MHz	PCI

Figure 2-8: PMC Connectors J17 and J19





2.3.8.1 PMC Connectors J17, and J19 Pinout

Table 2-18: PMC Connectors J17 and J19 Pinout

J17 (Jn1)				J19 (Jn2)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
TCK (pull-up)	1	2	-12V	+12V	1	2	TRST# (pull-down)
Ground	3	4	INTA#	TMS (pull-up)	3	4	TDO (NC)
INTB#	5	6	INTC#	TDI (pull-up)	5	6	Ground
BUSMODE1# (NC)	7	8	+5V	Ground	7	8	PCI-RSV (NC)
INTD#	9	10	PCI-RSV (NC)	PCI-RSV (NC)	9	10	PCI-RSV (NC)
Ground	11	12	3V3-AUX (NC)	BUSMODE2# (pull-up)	11	12	+3.3V
CLK	13	14	Ground	RST#	13	14	BUSMODE3# (GND)
Ground	15	16	GNT#	+3.3V	15	16	BUSMODE4# (GND)
REQ#	17	18	+5V	PCI-RSV (NC)	17	18	Ground
V (I/O)	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	Ground	21	22	AD[26]
AD[25]	23	24	Ground	AD[24]	23	24	+3.3V
Ground	25	26	C/BE[3]	IDSEL	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	Ground
V (I/O)	31	32	AD[17]	AD[16]	31	32	C/BE[2]#
FRAME#	33	34	Ground	Ground	33	34	PMC-RSV (NC)
Ground	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	Ground	37	38	STOP#
GND	39	40	LOCK#	PERR#	39	40	Ground
PCI-RSV (NC)	41	42	PCI-RSV (NC)	+3.3V	41	42	SERR#
PAR	43	44	Ground	C/BE[1]#	43	44	Ground
V (I/O)	45	46	AD[15]	AD[14]	45	46	AD[13]
AD[12]	47	48	AD[11]	M66EN	47	48	AD[10]
AD[09]	49	50	+5V	AD[08]	49	50	+3.3V
Ground	51	52	C/BE[0]#	AD[07]	51	52	PMC-RSV (NC)
AD[06]	53	54	AD[05]	+3.3V	53	54	PMC-RSV (NC)
AD[04]	55	56	Ground	PMC-RSV (NC)	55	56	Ground
V (I/O)	57	58	AD[03]	PMC-RSV (NC)	57	58	PMC-RSV (NC)
AD[02]	59	60	AD[01]	Ground	59	60	PMC-RSV (NC)
AD[00]	61	62	+5V	ACK64#	61	62	+3.3V
Ground	63	64	REQ64#	Ground	63	64	PMC-RSV (NC)



2.3.9 Debug Interface

The CP6001-V provides several onboard options for hardware and software debugging, such as:

- Two bicolor General Purpose LEDs (LED0..1), which indicate hardware failures, BIOS POST codes and port 80 user-configurable outputs
- A JTAG connector, J18, for programming and debugging the onboard logic
- An ITP700, processor JTAG connector, J24, for facilitating the debug and BIOS software development

2.3.10 CompactPCI Interface

The CP6001-V supports a flexibly configurable, hot swap CompactPCI interface. When the board is installed in the system slot, the interface is in the transparent mode, and when the board is installed in the peripheral slot, the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.3.10.1 Board Functionality when Installed in System Slot

In a system slot, the CP6001-V can communicate with all other CompactPCI boards through a 32-bit, 33/66 MHz interface.

The CP6001-V supports up to seven CompactPCI peripheral slots through a backplane.

2.3.10.2 Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

In this configuration, the communication is achieved via the two Gigabit Ethernet ports as defined in the PICMG 2.16 specification.

2.3.10.3 Packet Switching Backplane (PICMG 2.16)

The CP6001-V supports two Gigabit Ethernet ports on the J3 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16. The two ports are connected in the chassis via the CompactPCI Packet Switching Backplane to the Fabric slots "A" and "B".

The PICMG 2.16 feature can be used in the system slot and in the peripheral slot.

2.3.10.4 Hot Swap Support

To ensure that a board may be removed and replaced in a working bus without disturbing the system, the following additional features are required:

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- A hot swap LED to indicate that the board may be safely removed



2.3.10.5 Power Ramping

On the CP6001-V a special hot swap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates an onboard reset to put the board into a definite state.

2.3.10.6 Precharge

Precharge is provided on the CP6001-V by a resistor on each signal line (PCI bus), connected to a +1V reference voltage.

2.3.10.7 Handle Switch

A microswitch is situated in the extractor handle. The status of the handle is included in the on-board logic. The microswitch is connected to the onboard connector J10.

2.3.10.8 ENUM# Interrupt

If the board is operated in the system slot, the ENUM signal is an input.

2.3.10.9 Hot Swap LED

On the CP6001-V, a blue HS LED is provided, for example, to indicate the status of the shut-down process and when the board is ready for extraction.



2.3.11 CompactPCI Bus Connector

The complete CompactPCI connector configuration comprises three connectors, J1, J2 and J3 (optional). Their functions are as follows:

- J1/J2: 32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J3 (optional) with rear I/O interface functionality

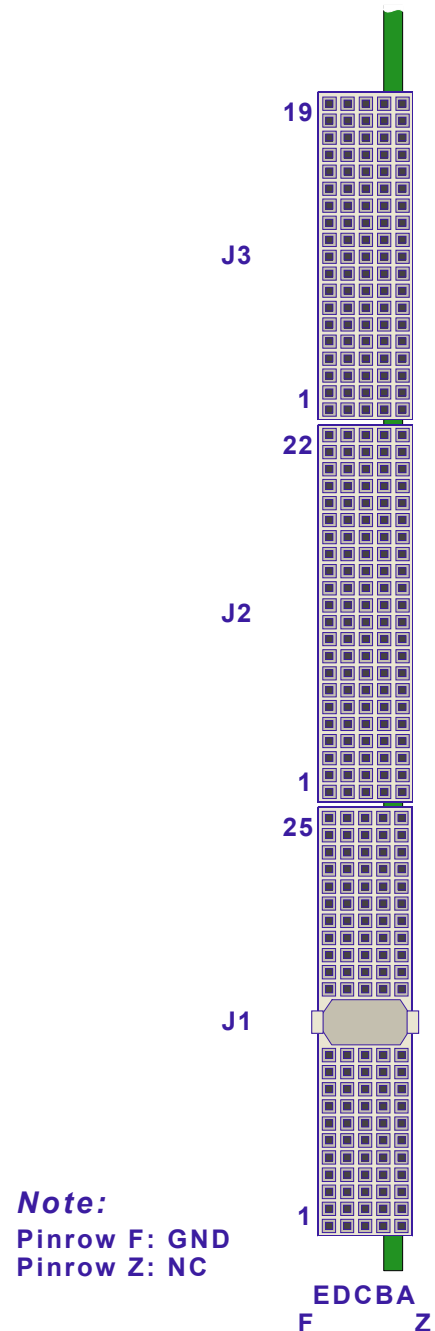
The CP6001-V is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.3.11.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating.

The CP6001-V supports universal PCI VI/O signaling voltages with one common termination resistor configuration and includes a PCI VI/O voltage detection circuit. If the PCI VI/O voltage is 5 V, the maximum supported PCI frequency is 33 MHz.

Figure 2-9: CPCI Connectors J1-J3





2.3.11.2 CompactPCI Connectors J1 and J2 Pinout

The CP6001-V is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-19: CompactPCI Bus Connector J1 System Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	NC	NC	GND	PERR#	GND
16	NC	DEVSEL#	PCI-X_CAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
14-12	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_Present#	3.3V	CLK0	AD[31]	GND
5	NC	RSV	RSV	RST#	GND	GNT0#	GND
4	NC	NC	Health#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

**Table 2-20: CompactPCI Bus Connector J1 Peripheral Slot Pinout**

PIN	Z	A	B	C	D	E	F
25	NC	5V	*	ENUM#	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	*	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	NC	NC	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_Present#	3.3V	*	*	GND
5	NC	NC	RSV	RST#**	GND	*	GND
4	NC	NC	Healthy#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6001-V is inserted in a peripheral slot.

** When the CP6001-V is inserted in a peripheral slot, the function of the RST# signal is maskable.



Table 2-21: 64-bit CompactPCI Bus Connector J2 System Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	GND	RSV	GND
19	NC	GND	GND	NC	NC	NC	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	NC	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	NC	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	NC	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	NC	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	NC	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	NC	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	NC	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	NC	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	NC	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	NC	C/BE[5]#	NC	V(I/O)	C/BE[4]#	PAR64	GND
4	NC	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

**Note ...**

The 64-bit CompactPCI signals are not used on the board, but all 64 control and address signals are terminated to V(I/O).

**Table 2-22: 64-bit CompactPCI Bus Connector J2 Peripheral Slot Pinout**

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	*	GND	RSV	RSV	RSV	GND
20	NC	*	GND	RSV	GND	RSV	GND
19	NC	GND	GND	NC	NC	NC	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	PRST#	*	*	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	*	*	GND
14	NC	*	*	*	GND	*	GND
13	NC	*	GND	V(I/O)	*	*	GND
12	NC	*	*	*	GND	*	GND
11	NC	*	GND	V(I/O)	*	*	GND
10	NC	*	*	*	GND	*	GND
9	NC	*	GND	V(I/O)	*	*	GND
8	NC	*	*	*	GND	*	GND
7	NC	*	GND	V(I/O)	*	*	GND
6	NC	*	*	*	GND	*	GND
5	NC	*	NC	V(I/O)	*	*	GND
4	NC	V(I/O)	RSV	*	GND	*	GND
3	NC	*	GND	*	*	*	GND
2	NC	*	*	SYSEN#	*	*	GND
1	NC	*	GND	*	*	*	GND

**Note ...**

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6001-V is inserted in a peripheral slot.



2.3.11.3 CompactPCI Rear I/O Connectors J3 Pinout

The CP6001-V board provides optional rear I/O connectivity for Gigabit Ethernet networking accordance with the PICMG 2.16.

The CP6001-V conducts all I/O signals through the rear I/O connectors J3.

Table 2-23: CompactPCI Rear I/O Connector J3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	NC	NC	NC	NC	NC	GND
18	NC	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	NC	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	NC	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	NC	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	NC	NC	NC	LPab:CT1	NC	NC	GND
13	NC	NC	NC	NC	NC	NC	GND
12	NC	NC	NC	NC	NC	NC	GND
11	NC	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	NC	GND
9	NC	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	NC	GND
6	NC	NC	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	NC	NC	GND
4	NC	NC	NC	NC	NC	NC	GND
3	NC	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	NC	GND
1	NC	NC	NC	NC	NC	NC	GND

Table 2-24: CompactPCI Rear I/O Connector J3 Signals

SIGNAL	DESCRIPTION
LPa	Rear I/O LAN Port D
LPb	Rear I/O LAN Port C
LPab	1.9 V for center tapping



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Chapter **3**

Installation



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3. Installation

The CP6001-V has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP6001-V. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.



Note...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.



ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.



3.2 CP6001-V Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP6001-V in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP6001-V in a system proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed.



Warning!

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP6001-V refer to Chapter 4. For the installation of CP6001-V specific peripheral devices, refer to the appropriate sub-chapters in Chapter 3.



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6001-V nor other system boards are physically damaged by the application of these procedures.

3. To install the CP6001-V perform the following:

1. Ensure that no power is applied to the system before proceeding.



Warning!

Even though power may be removed from the system, the CP6001-V front panel cables may have power applied which comes from an external source. In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damage or injuries resulting from failure to comply with the above.



Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.



3. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
4. Fasten the two front panel retaining screws.
5. Connect all external interfacing cables to the board as required.
6. Ensure that the board and all required interfacing cables are properly secured.

The CP6001-V is now ready for initial operation. Except for the BIOS, at this point there is no other software installed. For software installation and further operation of the CP6001-V, refer to appropriate CP6001-V software (BIOS, BSP, OS), application, and system documentation.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6001-V nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.



Warning!

Even though power may be removed from the system, the CP6001-V front panel cables may have power applied which comes from an external source. In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damage or injuries resulting from failure to comply with the above.

3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.



3.4 Hot Swap Procedures

The CP6001-V is designed for hot swap operation. When installed in the system slot it is capable of supporting peripheral board hot swapping. When installed in a peripheral slot, its hot swap capabilities depend on the type of backplane in use and the system controller's capabilities. The reason for this being that communication with the system controller requires either front panel Ethernet I/O or use of a packet switching backplane. In any event, hot swap is also a function of the application running on the CP6001-V.

3.4.1 Hot Swap of the Board Operated in the System Slot

Hot swapping of the CP6001-V itself when used as the system controller is possible, but will result in any event in a cold start of the CP6001-V and consequently a reinitialization of all peripheral boards. Exactly what transpires in such a situation is a function of the application and is not addressed in this manual. The user must refer to appropriate application documentation for applicable procedures for this case. In any event, the safety requirements above must be observed.

3.4.2 Hot Swap of the Board Operated in a Peripheral Slot

This procedure assumes that the system supports hot swapping, and that the replacement for the board to be hot swapped is configured hardware- and software-wise for operation in the application.

To hot swap the CP6001-V proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6001-V nor other system boards are physically damaged by the application of these procedures.

2. Unlock both board ejection handles ensuring that the bottom handle has activated the hot swap switch (this occurs with a very small amount of movement of the handle).



Note ...

What transpires at this time is a function of the application. If hot swap is supported by the application, then the blue HS LED should light up after a short time period. This indicates that the system has recognized that the CP6001-V is to be hot swapped and now indicates to the operator that hot swapping of the CP6001-V may proceed.

If the blue HS LED does not light up after a short time period, either the system does not support hot swap or a malfunction has occurred. In this event, the application is responsible for handling this situation and must provide the operator with appropriate guidance to remedy the situation.

3. After approximately 1 to 15 seconds, the blue HS LED should light up. If the LED lights up, proceed with the next step of this procedure. If the LED does not light up, refer to appropriate application documentation for further action.



4. Disconnect any interfacing cables that may be connected to the board.

**Warning!**

The CP6001 front panel cables may have power applied which comes from an external source. In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damage or injuries resulting from failure to comply with the above.

5. Unscrew the front panel retaining screws.

**Warning!**

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

6. Using the ejector handles, disengage the board from the backplane and carefully remove it from the system.
7. Dispose of the "old" board as required observing the safety requirements indicated in Chapter 3.1.
8. Obtain the replacement CP6001-V board.

**Warning!**

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

9. Carefully insert the "new" board into the "old" board slot until it makes contact with the backplane connectors.
10. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
11. Fasten the front panel retaining screws.
12. Connect all required interfacing cables to the board. Hot swap of the CP6001-V is now complete.

**Warning!**

The CP6001 front panel cables may have power applied which comes from an external source. In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

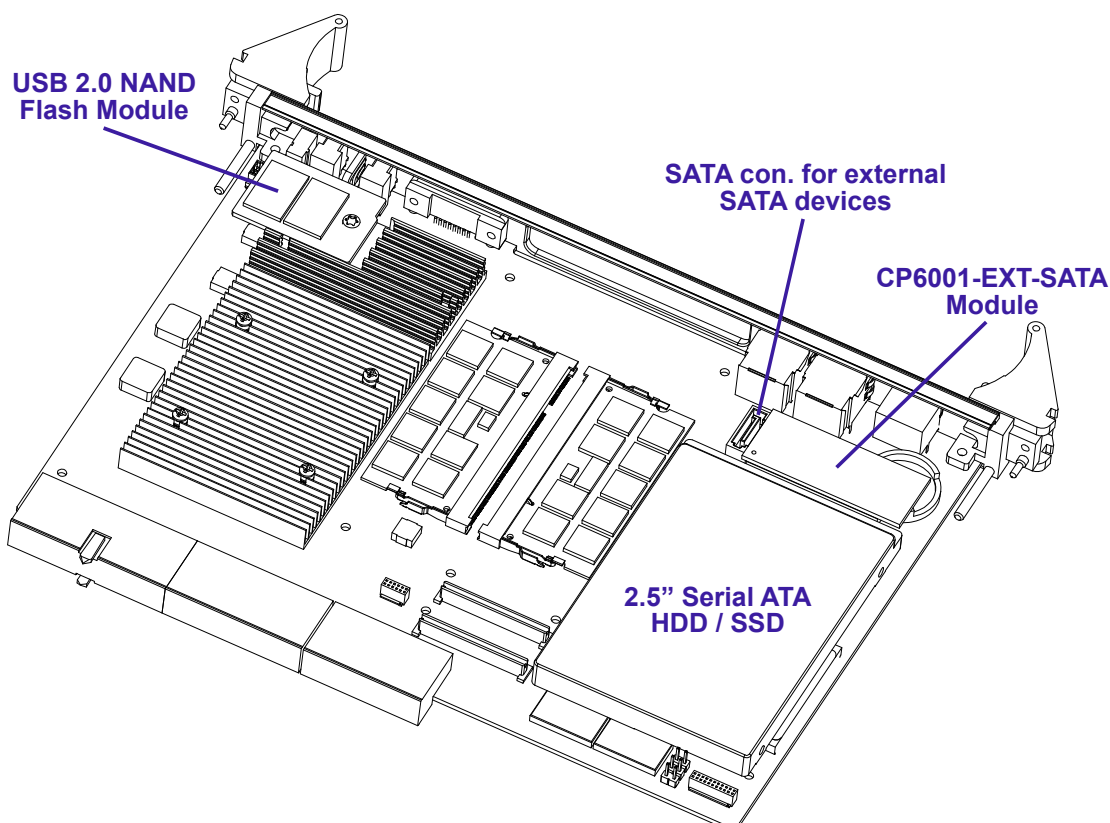
It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damage or injuries resulting from failure to comply with the above.

3.5 Installation of CP6001-V Peripheral Devices

The CP6001-V is designed to accommodate various peripheral devices, such as USB devices, Serial ATA devices, PMC devices, rear I/O devices, etc. The following figure shows the placement of the USB 2.0 NAND Flash module and the CP6001-EXT-SATA module, which is required to connect an onboard HDD/SSD to the CP6001-V.

Figure 3-1: Connecting a Peripheral Device to the CP6001-V



The following chapters provide information regarding installation aspects of peripheral devices.

3.5.1 USB Device Installation

The CP6001-V supports all USB Plug and Play computer peripherals (e.g. keyboard, mouse, printer, etc.).



Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.



3.5.2 USB 2.0 NAND Flash Module Installation

A USB 2.0 NAND Flash module may be connected to the CP6001-V via the onboard USB 2.0 NAND Flash connector, J11.

This optionally available module must be physically installed on the CP6001-V prior to installation of the CP6001-V in a system.

During installation it is necessary to ensure that the USB 2.0 NAND Flash module is properly seated in the onboard USB 2.0 NAND Flash connector, i.e. the pins are aligned correctly and not bent. To secure the USB 2.0 NAND Flash module to the CP6001-V, tighten the fastening screw.

Before putting the CP6001-V into operation, ensure that the boot priority is configured as required for the application.

3.5.3 Installation of External Serial ATA Devices

The following information pertains to external SATA devices which may be connected to the CP6001-V via normal cabling.

Some symptoms of incorrectly installed SATA devices are:

- Device on a SATA channel does not spin up: check power cables and cabling. May also result from a bad power supply or SATA device.
The SATA connector on the CP6001-V provides only a data connection. The power for this device must be supplied by a separate connector. For further information, refer to the respective documentation of the device.
- SATA device fail message at boot-up: may be a bad cable or lack of power going to the drive.

3.5.4 Onboard 2.5" HDD/SSD Installation

One 2.5" SATA HDD/SSD may be directly connected to the board via J13 and the adapter module CP6001-ETX-SATA. This module is required to provide Serial ATA interfacing to the HDD/SSD. For further information regarding the CP6001-ETX-SATA module, refer to Appendix A.

3.6 PMC Module Installation

The CP6001-V supports the installation of a PMC module via the connectors J17 and J19.

For the initial installation and standard removal of all PMC modules refer to the documentation provided with the module.



Prior to installation or removal, ensure that the safety requirements indicated in Chapter 3.1 of this user guide are observed. Particular attention must be paid to the warning regarding the heat sink!

**Warning!**

Always ensure that the board's PMC PCI signaling environment and the PMC card's PCI signaling environment are compatible.

The CP6001-V is delivered with 3.3V PMC PCI signaling environment configuration. If 5V PMC PCI signaling environment is required, please contact Kontron for further assistance.

Failure to comply with the instruction above may result in improper operation or damage to the PMC module.

3.6.1 Battery

The CP6001-V is provided with a 3.0 V "coin cell" lithium battery for the RTC.

To replace the battery, proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR2025.

**Note ...**

The user must be aware that the battery's operational temperature range is less than that of the CP6001-V's storage temperature range.

For exact range information, refer to the battery manufacturer's specifications.

**Note ...**

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.

To ensure that the lifetime of the battery has not been exceeded, it is recommended to exchange the battery after 4 - 5 years.

3.7 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.



Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

**Note ...**

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.



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Chapter

4

Configuration



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4. Configuration

4.1 Jumper Description

4.1.1 Clearing BIOS CMOS Setup

If the system does not boot (due to, for example, the wrong BIOS configuration or wrong password setting), the CMOS setting may be cleared by using the solder jumper JP1.

Procedure for clearing the CMOS setting:

- Power down the system
- Set the solder jumper JP1 to closed
- Power up the system
- Power down the system again
- Reset the solder jumper JP1 to the normal position (open)
- Reboot the system

Table 4-1: Clearing BIOS CMOS Setup

JP1	DESCRIPTION
<i>Open</i>	<i>Normal boot using the CMOS settings</i>
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by using italic bold.

4.1.2 Shorting Chassis GND (Shield) to Logic GND

The front panel and the front panel connectors are isolated from the logic ground by means of capacitors. If it is necessary to connect the logic GND with the chassis GND, this should be done on the backplane, not on the board itself (see the PICMG CompactPCI Specification 2.0 R3.0, section 3.6).

For further information, refer to the *Kontron CompactPCI Backplane Manual* on the Kontron web site.

4.1.3 General Purpose Jumper

The CP6001-V provides one general purpose jumper, J20, which is reserved for future use.

4.1.4 CompactPCI Interface Configuration

The CP6001-V provides one jumper, J21, for CompactPCI clock configuration. This jumper is used to force the CompactPCI interface to operate at 33 MHz even when the system is able to operate at higher clock rates.

Table 4-2: CompactPCI Clock Configuration

J21	DESCRIPTION
<i>Open</i>	<i>PCI 33 MHz / 66 MHz auto detection via the CompactPCI backplane</i>
Closed	PCI frequency configured to 33 MHz

The default setting is indicated by using italic bold.



4.1.5 Global Write Protection

The CP6001-V provides one jumper, J22, used to prevent onboard memory devices from unauthorized or accidental write cycles. On the CP6001-V, only the BIOS Flash can be write-protected via this jumper.

Table 4-3: CompactPCI Clock Configuration

J22	DESCRIPTION
<i>Open</i>	<i>Write protection disabled</i>
Closed	Write protection enabled

The default setting is indicated by using italic bold.

4.2 I/O Address Map

The following table indicates the CP6001-V-specific registers.

Table 4-4: I/O Address Map

ADDRESS	DEVICE
0x080	POST Code Low Byte Register (POSTL)
0x081	POST Code High Byte Register (POSTH)
0x280	Status Register 0 (STAT0)
0x281	Status Register 1 (STAT1)
0x282	Reserved
0x283	Control Register 1 (CTRL1)
0x284	Device Protection Register (DPROT)
0x285	Reset Status Register (RSTAT)
0x286	Board Interrupt Configuration Register (BICFG)
0x287	Reserved
0x288	Board ID Register (BID)
0x289	Board and PLD Revision Register (BREV)
0x28A	Geographic Addressing Register (GEOAD)
0x28B	Delay Timer Register (DTIM)
0x28C	Watchdog Timer Control Register (WTIM)
0x28D - 0x28F	Reserved
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292 - 0x29F	Reserved



4.3 CP6001-V-Specific Registers

The following registers are special registers which the CP6001-V uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.



Note ...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.3.1 Status Register 0 (STAT0)

The Status Register 0 holds general/common status information.

Table 4-5: Status Register 0 (STAT0)

REGISTER NAME		STATUS REGISTER 0 (STAT0)		
ADDRESS		0x280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	HSLS	Hot swap handle status: 0 = Hot swap handle in closed position 1 = Hot swap handle in open position	N/A	R
6	BBEI	BIOS boot end indication: 0 = BIOS is booting 1 = BIOS boot is finished	0	R
5 - 4	BFSS	Boot Flash selection status: 00 = Boot Flash 0 active 01 = Reserved 10 = External boot Flash active 11 = Reserved	N/A	R
3 - 0	Res.	Reserved	0000	R

4.3.2 Status Register 1 (STAT1)

The Status Register 1 holds board-specific status information.

Table 4-6: Status Register 1 (STAT1)

REGISTER NAME		STATUS REGISTER 1 (STAT1)		
ADDRESS		0x281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	C66EN	CPCI PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
6	CVIO	CPCI backplane VI/O voltage configuration: 0 = 3.3V VI/O voltage 1 = 5V VI/O voltage	N/A	R
5	P66EN	PMC PCI speed (M66EN signal): 0 = 33 MHz	0	R
4	Res.	Reserved	0	R
3	CSYS	CPCI system slot identification (SYSEN signal): 0 = Installed in a system slot 1 = Installed in a peripheral slot	N/A	R
2	CENUM	CPCI system enumeration (ENUM signal): 0 = Indicates the insertion or removal of a hot swap system board 1 = No hot swap event	N/A	R
1	CFAL	CPCI power supply status (FAL signal): 0 = Power supply failure 1 = Power in normal state	N/A	R
0	CDEG	CPCI power supply status (DEG signal): 0 = Power derating 1 = Power in normal state	N/A	R

4.3.3 Control Register 1 (CTRL1)

The Control Register 1 holds board-specific control information.

Table 4-7: Control Register 1 (CTRL1)

REGISTER NAME		CONTROL REGISTER 1 (CTRL1)		
ADDRESS		0x283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4	CRST	CPCI reset when the board is used in a peripheral slot: 0 = Disable CPCI reset to board 1 = Enable CPCI reset to board	0	R/W
3 - 0	Res.	Reserved	0000	R



4.3.4 Device Protection Register (DPROT)

The Device Protection Register holds the write protect signals for Flash devices.

Table 4-8: Device Protection Register (DPROT)

REGISTER NAME		DEVICE PROTECTION REGISTER (DPROT)		
ADDRESS		0x284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	GWP	Global write protection: 0 = Memory devices not write-protected (Boot Flash) 1 = Memory devices write-protected (Boot Flash) This bit indicates the status of the global write protection jumper, J22.	N/A	R
6 - 1	Res.	Reserved	000000	R
0	BFWP	Boot Flash write protection: 0 = Boot Flash not write-protected 1 = Boot Flash write-protected Writing a '1' to this bit sets the bit. If the bit is set, it cannot be cleared.	0	R/W

4.3.5 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 4-9: Reset Status Register (RSTAT)

REGISTER NAME		RESET STATUS REGISTER (RSTAT)		
ADDRESS		0x285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset status: 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears the bit.	N/A	R/W
6 - 3	Res.	Reserved	0000	R
2	FPRS	Front panel push button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.	0	R/W
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CPCI reset input 1 = System reset generated by CPCI reset input Writing a '1' to this bit clears the bit.	0	R/W
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W



Note ...

The reset status register is set to the default values by power-on reset, not by PCI reset.

4.3.6 Board Interrupt Configuration Register (BICFG)

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing for the Watchdog. If the Watchdog Timer fails, it can generate an IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force the software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Table 4-10: Board Interrupt Configuration Register (BICFG)

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER (BICFG)		
ADDRESS		0x286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	CFICF	CPCI fail signal interrupt configuration (FAL signal): 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved	00	R
5	CEICF	CPCI enumeration signal to IRQ5 routing (ENUM signal): 0 = Disabled 1 = Enabled	0	R/W
4	CDICF	CPCI derate signal to IRQ5 routing (DEG signal): 0 = Disabled 1 = Enabled	0	R/W
3 - 2	Res.	Reserved	00	R
1 - 0	WICF	Watchdog interrupt configuration 00 = Disabled 01 = IRQ5 11 = Reserved	00	R/W

4.3.7 Board ID Register (BID)

This register provides the board's coded ID, which is unique for the CP6001-V.

Table 4-11: Board ID Register (BID)

REGISTER NAME		BOARD ID REGISTER (BID)		
ADDRESS		0x288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BID	Board identification 0xB0 = CP6001-V	0xB0	R



4.3.8 Board and PLD Revision Register (BREV)

The Board and PLD Revision Register signals to the software when differences in the board and the Programmable Logic Device (PLD) require different handling by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each change in hardware as development continues.

Table 4-12: Board and PLD Revision Register (BREV)

REGISTER NAME		BOARD AND PLD REVISION REGISTER (BREV)		
ADDRESS		0x289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	BREV	Board revision	N/A	R
3 - 0	PREV	PLD revision	N/A	R

4.3.9 Geographic Addressing Register (GEOAD)

The Geographic Addressing Register describes the CompactPCI geographic addressing signals.

Table 4-13: Geographic Addressing Register (GEOAD)

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER (GEOAD)		
ADDRESS		0x28A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4 - 0	GA	CPCI geographic address	N/A	R

4.3.10 Delay Timer Register (DTIM)

The delay timer enables the user to realize short, reliable delay times. It runs by default and does not start again on its own. It can be restarted at anytime by writing anything other than a '0' to the Delay Timer Register. The hardware delay timer provides a set of outputs for defined elapsed time periods. The timer outputs reflected in the Delay Timer Register are set consecutively and remain set until the next restart is triggered again.

Table 4-14: Delay Timer Register (DTIM)

REGISTER NAME		DELAY TIMER REGISTER (DTIM)																													
ADDRESS		0x28B																													
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS																											
7 - 0	DTC	<p>The hardware delay timer is operated via one simple 8-bit control/status register. During normal operation, each of the 8 bits reflects a timer output which means defined elapsed time period after the last restart according to the following bit mapping:</p> <table><thead><tr><th>DTC[7:0]</th><th>Value</th><th>Accuracy</th></tr></thead><tbody><tr><td>Bit 7:</td><td>1 ms</td><td>< + 0.04%</td></tr><tr><td>Bit 6:</td><td>500 μs</td><td>< + 0.08%</td></tr><tr><td>Bit 5:</td><td>250 μs</td><td>< + 0.16%</td></tr><tr><td>Bit 4:</td><td>100 μs</td><td>< + 0.4%</td></tr><tr><td>Bit 3:</td><td>50 μs</td><td>< + 0.8%</td></tr><tr><td>Bit 2:</td><td>10 μs</td><td>< + 4%</td></tr><tr><td>Bit 1:</td><td>5 μs</td><td>< + 8%</td></tr><tr><td>Bit 0:</td><td>1 μs</td><td>< + 40%</td></tr></tbody></table>	DTC[7:0]	Value	Accuracy	Bit 7:	1 ms	< + 0.04%	Bit 6:	500 μs	< + 0.08%	Bit 5:	250 μs	< + 0.16%	Bit 4:	100 μs	< + 0.4%	Bit 3:	50 μs	< + 0.8%	Bit 2:	10 μs	< + 4%	Bit 1:	5 μs	< + 8%	Bit 0:	1 μs	< + 40%	0x00	R/W
DTC[7:0]	Value	Accuracy																													
Bit 7:	1 ms	< + 0.04%																													
Bit 6:	500 μs	< + 0.08%																													
Bit 5:	250 μs	< + 0.16%																													
Bit 4:	100 μs	< + 0.4%																													
Bit 3:	50 μs	< + 0.8%																													
Bit 2:	10 μs	< + 4%																													
Bit 1:	5 μs	< + 8%																													
Bit 0:	1 μs	< + 40%																													

Since the timer width and thus the availability of outputs varies over different implementations, it is necessary to be able to determine the timer capability. Therefore, writing a '0' to the Delay Timer Register followed by reading indicates the timer capability (not the timer outputs). For example, writing 0x00 and then reading 0xFF results in a 8-bit wide timer register. This status register mode can be switched off to normal timer operation by writing anything other than a '0' to this register.



4.3.11 Watchdog Timer Control Register (WTIM)

The CP6001-V has one Watchdog Timer provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the Watchdog Timer within a set time period results in a system reset or an interrupt. The interrupt mode can be configured via the Board Interrupt Configuration Register (0x286).

There are four possible modes of operation involving the Watchdog Timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register (0x282) must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode/timeout changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a '1' to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to '1'. What transpires after this depends on the mode selected.

The four operational Watchdog Timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a '1' to the WTR bit. In the event a timeout occurs, the WTE bit is set to '1'. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a '1' to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.



Table 4-15: Watchdog Timer Control Register (WTIM)

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER (WTIM)		
ADDRESS		0x28C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog Timer expired status bit 0 = Watchdog Timer has not expired 1 = Watchdog Timer has expired. Writing a '1' to this bit resets it to 0.	0	R/W
6 - 5	WMD	Watchdog Mode 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable/Watchdog trigger control bit: 0 = Watchdog Timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog Timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog Timer is enabled, it will indicate a '1'. 1 = Watchdog Timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3 - 0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = reserved 1101 = reserved 1110 = reserved 1111 = reserved The nominal timeout period is 5% longer than the above-stated values.	0000	R/W



4.3.12 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel LEDs.

Table 4-16: LED Configuration Register (LCFG)

REGISTER NAME		LED CONFIGURATION REGISTER (LCFG)		
ADDRESS		0x290		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	Res.	Reserved	0000	R
3 - 0	LCON	Front panel LEDs Configuration: 0000 = POST ¹⁾ 0001 = General Purpose Mode ²⁾ 0010 - 1111 = Reserved	0000	R/W

Regardless of the selected configuration, the front panel LEDs are used to signal a number of fatal onboard hardware errors, such as:

LED0: BIOS boot fail (red)
 LED1: BIOS boot fail (red)
 WD LED: Watchdog enabled (green) and Watchdog expired (red)
 TH LED: Thermal alarm (red blinking), thermal shutdown (amber)

¹⁾ In BIOS POST mode (default), the LEDs build a binary vector to display BIOS POST code during the BIOS boot phase. In doing so, the higher 4-bit nibble of the 8-bit BIOS POST code is displayed followed by the lower nibble followed by a pause. BIOS POST code is displayed in general in green color.

LED0: POST bit 3 and bit 7 (green)
 LED1: POST bit 2 and bit 6 (green)
 WD LED: POST bit 1 and bit 5 (green)
 TH LED: POST bit 0 and bit 4 (green)

For further information on reading the 8-Bit BIOS POST Code, refer to Chapter 2.3.2.

²⁾ Configured for General Purpose Mode, the LEDs are dedicated to functions as follows:

LED0: LED 0, controlled by HOST (red/green)
 LED1: LED 1, controlled by HOST (red/green)
 WD LED: Watchdog enabled (green) and Watchdog expired (red)
 TH LED: Thermal alarm (red blinking), thermal shutdown (amber)



4.3.13 LED Control Register (LCTRL)

The LED Control Register enables the user to switch on and off the General Purpose LEDs.

Table 4-17: LED Control Register (LCTRL)

REGISTER NAME		LED CONTROL REGISTER (LCTRL)		
ADDRESS		0x291		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	LCMD	LED command: 0000 = Get LED 0 0001 = Get LED 1 0010 - 0111 = Reserved 1000 = Set LED 0 1001 = Set LED 1 1010 - 1111 = Reserved	0000	R/W
3 - 0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Amber 0100 - 1111 = Reserved	000	R/W



Note ...

This register can only be used if the General Purpose LEDs indicated in the “LED Configuration Register” (Table 4-16) are configured in General Purpose Mode.



Chapter

5

Power Considerations



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5. Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP6001-V system environment.

5.1.1 CP6001-V Baseboard

The CP6001-V baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP6001-V should be carefully tested to ensure compliance with these ratings.

Table 5-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V



Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP6001-V is not guaranteed to function if the board is not operated within the prescribed limits.

Table 5-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.	Only for PMC



5.1.2 Backplane

Backplanes to be used with the CP6001-V must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs. It is recommended to use only backplanes which have at least two power planes for the 3.3 V and +5 V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

5.1.3 Power Supply Units

Power supplies for the CP6001-V must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP6001-V has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for backplane input line resistance variations due to temperature changes, etc.



Note ...

Non-industrial ATX PSUs may require a greater minimum load than a single CP6001-V is capable of creating. When a PSU of this type is used, it may not power up correctly and cause the CP6001-V to hang up. The solution is to use an industrial PSU or to add more load to the system.

The start-up behavior of CPCI and PCI (ATX) power supplies is critical for all new CPU boards. These boards require a defined power sequence and start-up behavior of the power supply. For information on the required behavior refer to the power supply specifications on the formfactors.org web site and to the PICMG CompactPCI specification on the picmgeu.org web site.

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP6001-V.

- Beginning at 10% of the nominal output voltage, the voltage must rise within $> 0.1 \text{ ms}$ to $< 20 \text{ ms}$ to the specified regulation range of the voltage. Typically: $> 5 \text{ ms}$ to $< 15 \text{ ms}$.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal V_{out} .



5.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CPCI specification (PICMG 2.0 R3.0). The recommended measurement point for the voltage is the CPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 5-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	--
+12 V	+12 VDC	+5%/-5%	240 mV	Required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
VI/O (PCI) voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	--
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.



5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP6001-V baseboard and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and the power specifications for the CP6001-V board and its accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU, and the other for the hard disk. The operating systems used were DOS, Linux and Windows® XP. All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on the processor activity.



Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 10%.

The power consumption was measured using the following processor:

- Intel® Celeron® M processor 440, 1.86 GHz, 533 MHz FSB, 1 MB L2 cache

with the following operating systems:

- DOS
This operating system has no power management support and provides a very simple method to verify the measured power consumption values.
- Linux/Windows® XP, IDLE Mode
With these operating systems both processor cores were in IDLE state.

and under the following testing conditions:

- CP6001-V's Thermal Design Power (TDP) at 75%
These values represent the "typical" maximum power dissipation reached under OS-controlled applications.
- CP6001-V's Thermal Design Power (TDP) at 100%
These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores. 100% TDP is unlikely to be reached in real applications.

The following tables indicate the power consumption of the CP6001-V with 1 GB DDR2 SDRAM in dual-channel mode. For measurements made with the Linux and Windows® XP operating systems, the VGA resolution was 1280 x 1024 pixels.

**Table 5-4: Power Consumption: CP6001-V with DOS**

POWER	Celeron® M 440 1.86 GHz 1GB SO-DIMM DDR2	Celeron® M 440 1.86 GHz 2 GB / 4 GB SO-DIMM DDR2
12 V	50 mW	50 mW
5 V	16 W	16 W
3.3 V	6.3 W	6.6 W
Total	22.35 W	22.65 W

Table 5-5: Power Consumption: CP6001-V with Linux/Win. XP in IDLE Mode

POWER	Celeron® M 440 1.86 GHz 1GB SO-DIMM DDR2	Celeron® M 440 1.86 GHz 2 GB / 4 GB SO-DIMM DDR2
12 V	50 mW	50 mW
5 V	10 W	10 W
3.3 V	6.6 W	6.6 W
Total	16.65 W	16.65 W

Table 5-6: Power Consumption: CP6001-V's TDP at 75%

POWER	Celeron® M 440 1.86 GHz 1GB SO-DIMM DDR2	Celeron® M 440 1.86 GHz 2 GB / 4 GB SO-DIMM DDR2
12 V	50 mW	50 mW
5 V	15 W	18 W
3.3 V	6.6 W	6.6 W
Total	21.65 W	24.65 W

Table 5-7: Power Consumption: CP6001-V's TDP at 100%

POWER	Celeron® M 440 1.86 GHz 1GB SO-DIMM DDR2	Celeron® M 440 1.86 GHz 2 GB / 4 GB SO-DIMM DDR2
12 V	50 mW	50 mW
5 V	21.5 W	21.5 W
3.3 V	6.6 W	6.6 W
Total	28.15 W	28.15 W



5.2.1 Power Consumption of the CP6001-V Accessories

The following table indicates the power consumption of the CP6001-V accessories.

Table 5-8: Power Consumption of CP6001-V Accessories

MODULE	POWER 5 V	POWER 3.3 V AVERAGE
Keyboard	100 mW	--
CompactFlash	--	100 mW - 300 mW
USB 2.0 NAND Flash module	325 mW - 400 mW	--
2.5" HDD/SSD	refer to the respective datasheet	

5.2.2 Power Consumption of the Gigabit Ethernet Controller

The following table indicates the power consumption of the Intel® 82574L GbE controller.

Table 5-9: Power Consumption of the Gigabit Ethernet Controller

ETHERNET PORT	SPEED	POWER
Intel® 82574L, one Ethernet port plugged	1000 Mb/s	approx. 0.5 W

5.3 Start-Up Currents of the CP6001-V

The following table indicates the basic start-up currents of the CP6001-V during the first 2-3 seconds after power has been applied (power-on or hot-swap insertion).

Table 5-10: Start-Up Currents of the CP6001-V

POWER		Celeron® M 440 1.86 GHz
5 V	peak	7.0 A
	average	2.0 A
3.3 V	peak	6.0 A
	average	3.2 A



5.4 Power Available for PMC Devices

The following table indicates the power made available by the CP6001-V to PMC devices.

Table 5-11: Maximum Output Power Limits

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
+3.3 V	2.27 A	4.0 A
+5 V	1.5 A	3.0 A
+12 V	0.5 A	0.8 A
-12 V	0.1 A	0.2 A



Note ...

A maximum power of 7.5 W is available on the pins of the PMC connectors J17 and J19, which provide a voltage of 3.3 V or 5 V. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5 W can be arbitrarily divided on the 3.3 V and 5 V voltage lines.

The -12 V voltage line is only required for operation of PMC modules. Their availability depends on the power supply.



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Chapter

6

Thermal Considerations



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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing CP6001-V applications.

6.1 Board Internal Thermal Monitoring

To ensure optimal operation and long-term reliability of the CP6001-V, all onboard components must remain within the maximum temperature specifications. The most critical components on the CP6001-V are the processor and the chipset. Operating the CP6001-V above the maximum operating limits will result in permanent damage to the board.

The CP6001-V includes the following sensors to measure the CPU temperature and regulate the board's power consumption.

- Thermal sensors integrated in the processor
- Temperature sensor integrated in the Super I/O

The temperature sensor integrated on the Super I/O is accessible via the host. For information on the temperature sensor integrated in the CPU, refer to Chapter 6-2.

6.2 Processor Thermal Monitoring and Regulation

The Intel® Celeron® M 440 processor includes the following on-die temperature sensors:

- Digital Thermal Sensor (DTS)
- Thermal Monitor 1 (TM1) Sensor
- Catastrophic Cooling Failure Sensor

Via the Digital Thermal Sensor (DTS), the BIOS or the application software can measure the processor die temperature.

The Thermal Monitor 1 (TM1) Sensor and the Catastrophic Cooling Failure Sensor are not accessible. They serve for protecting the processor from overheating. These sensors are integrated in the processor and work without any interoperability of the BIOS or the software application. The thermal monitor function utilizes the thermal control circuit to regulate the processor temperature. It is enabled in the BIOS and allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

The maximum die temperatures for all processor types is as follows:

- Intel® Celeron® M 440: 100°C

6.2.1 Digital Thermal Sensor (DTS)

The processor includes one on-die Digital Thermal Sensors (DTS) that can be read via an internal register of the processor (no I/O interface). The Digital Thermal Sensor provides the preferred method of reading the processor die temperature since it is located much closer to the hottest portions of the die and can thus more accurately track the die temperature.

6.2.2 Thermal Monitor 1 (TM1)

The Thermal Monitor 1 (TM1) Sensor controls the processor temperature and power consumption by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature (100°C).



When TM1 is enabled and a high temperature situation exists, the processor clock is modulated using duty cycles. Once the temperature has dropped below the maximum operating temperature, the Thermal Control Circuit goes inactive.

The temperature at which TM1 activates the Thermal Control Circuit is neither user-configurable nor software-visible.

TM1 does not require any additional hardware, software drivers, or interrupt handling routines. This function can be enabled and disabled in the BIOS.

**Note ...**

The TH LED on the front panel shows the status of the internal thermal supervision if POST code configuration is disabled in the BIOS.

6.2.3 Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating. The Catastrophic Cooling Failure Sensor threshold is set well above the maximum operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 125°C. Once activated, the event remains latched until the CP6001-V undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the BIOS. It is always enabled to ensure that the processor is protected in any event.

**Note ...**

When the TH LED on the front panel is lit amber after a successful boot-up and the POST code configuration is disabled, it indicates that the processor die temperature is above 125°C.

6.3 External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the CP6001-V is equipped with a heat sink. Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed. The physical size, shape, and construction of the heat sink ensure the lowest possible thermal resistance. In addition, the CP6001-V has been specifically designed to efficiently support forced airflow as found in modern CompactPCI systems. The CP6001-V must not be operated without the minimum required forced airflow.



6.3.1 Thermal Characteristic Graph

The thermal characteristic graph shown in this section illustrates the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagram is intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version is provided. There is one curve representing upper level working points based on maximum level of CPU utilization. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 2.5 m/s is a typical value for a standard *Kontron* ASM rack (6U CompactPCI rack with a 1U cooling fan tray). For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor and chipset junction temperature must never exceed the specified limit for the involved processor and chipset.

TDP curve

- 100% TDP curve
This load complies with the maximum thermal design power (TDP) indicated in Chapter 5.2 Power Consumption, Table 5-7. 100% TDP can be achieved through the use of specific tools to heat up the CPU but 100% TDP is unlikely to be reached in real applications.

How to read the diagram

Choose a specific working point indicated in TDP percentage. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must not be less than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in m³/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m³/h; 1 m³/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

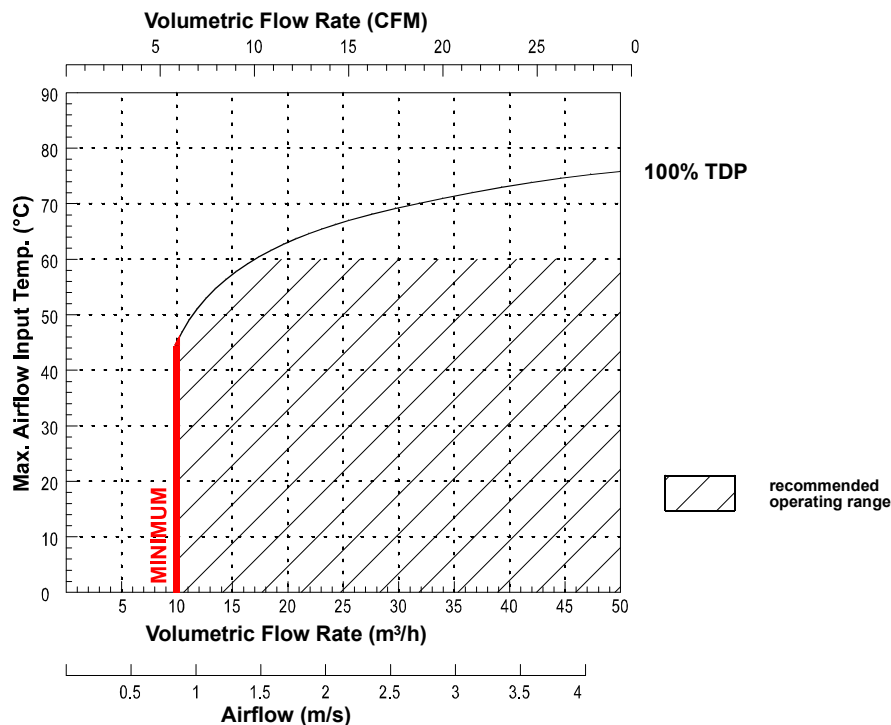
The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps



The following figure illustrates the operational limits of the CP6001-V taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot.

Figure 6-1: Oper. Limits for the CP6001-V with Intel® Celeron® M 440, 1.86 GHz



6.3.2 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP6001-V must also be considered. Devices such as hard disks, PMC modules, etc. which are directly attached to the CP6001-V must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.



Warning!

As Kontron assumes no responsibility for any damage to the CP6001-V or other equipment resulting from overheating of the CPU or any other board components, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6001-V complies with the thermal considerations set forth in this document.



Appendix



CP6001-V-MK2.5SATA



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A. CP6001-V-MK2.5SATA Assembly Kit

The optional CP6001-V-MK2.5SATA assembly kit includes one CP6001-EXT-SATA module and the necessary components required for mounting the module on the CP6001-V.

A.1 CP6001-EXT-SATA Module Overview

The CP6001-EXT-SATA module has been designed for use with the CP6001-V board from Kontron and enables the user to connect an onboard 2.5" Serial ATA HDD or SSD to the CP6001-V.

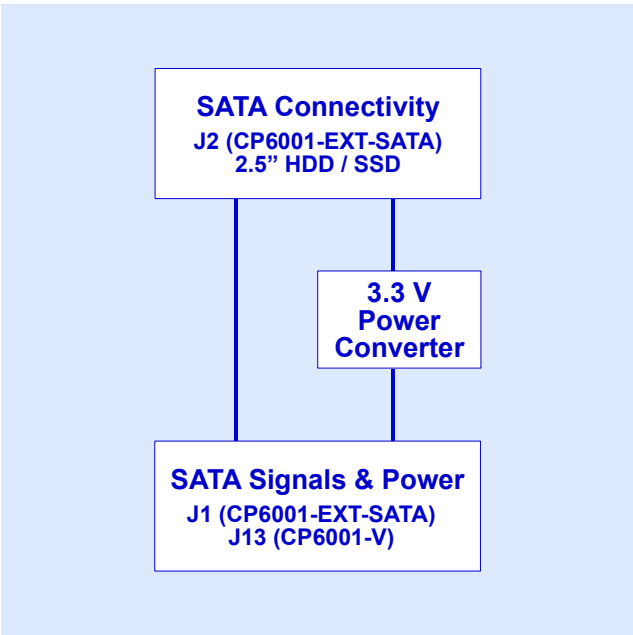
A.2 Technical Specifications

Table A-1: CP6001-EXT-SATA Main Specifications

CP6001-EXT-SATA		SPECIFICATIONS
Interfaces	Board-to-Board Connectors	One 12-pin, male, board-to-board connector, J1
	Serial ATA Connector	One 22-pin Serial ATA connector, J2
General	Power Consumption	3.3 V or 5 V, depending on the HDD/SSD Current 2.5" Serial ATA HDDs do not use 3.3 V.
	Temperature Range	Operating temp.: 0°C to +60°C Storage temp.: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	54 mm x 27.5 mm
	Board Weight	ca.6 grams (without HDD/SSD)

A.3 CP6001-EXT-SATA Functional Block Diagram

Figure A-1: CP6001-EXT-SATA Functional Block Diagram

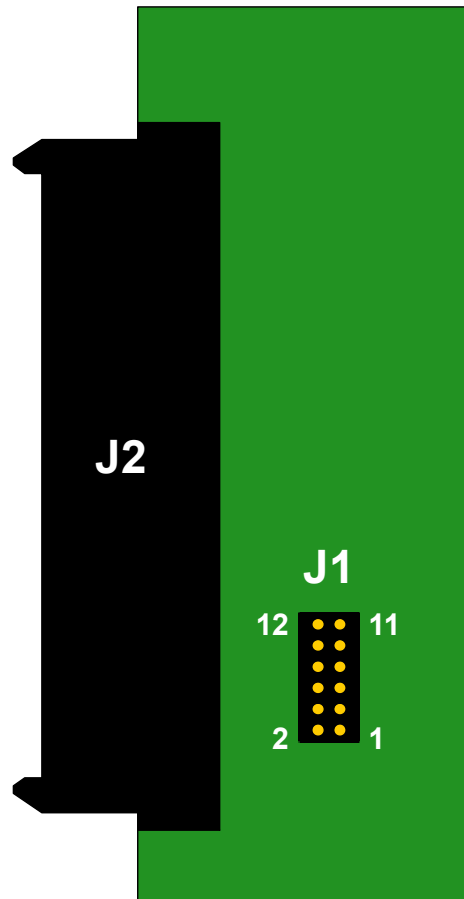




A.4 CP6001-EXT-SATA Module Layout

The CP6001-EXT-SATA module includes one board-to-board connector, J1, and one SATA connector, J2.

Figure A-2: CP6001-EXT-SATA Module Layout





A.5 **Module Interfaces**

A.5.1 **Board-to-Board Connector J1**

The board-to-board connector, J1, on the CP6001-EXT-SATA module is connected to the SATA extension connector, J13, on the CP6001-V.

Table A-2: Board-to-Board Connector J1 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	SATA_RX-	Differential Receive -	O
2	GND	Ground signal	--
3	SATA_RX+	Differential Receive +	O
4	GND	Ground signal	--
5	GND	Ground signal	--
6	5V	5V power	--
7	SATA_TX-	Differential Transmit -	I
8	GND	Ground signal	--
9	SATA_TX+	Differential Transmit +	I
10	GND	Ground signal	--
11	GND	Ground signal	--
12	5V	5V power	--



A.5.2 SATA Connector J2

The SATA connector, J2, on the CP6001-EXT-SATA module is connected to the 2.5" SATA HDD mounted on the CP6001-V. The SATA connector is divided into two segments, a signal segment and a power segment.

Figure A-3: SATA Connector J2

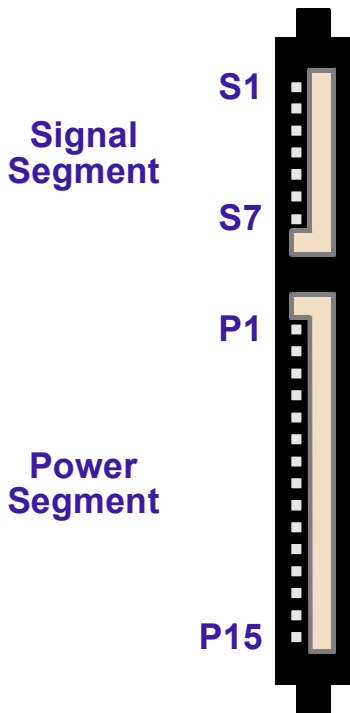


Table A-3: SATA Connector J2 Pinout

PIN	SIGNAL	FUNCTION	I/O
Signal Segment Key			
S1	GND	Ground signal	--
S2	SATA_TX+	Differential Transmit+	I
S3	SATA_TX-	Differential Transmit-	I
S4	GND	Ground signal	--
S5	SATA_RX-	Differential Receive-	O
S6	SATA_RX+	Differential Receive+	O
S7	GND	Ground signal	--
Signal Segment "L"			
Central Connector Polarizer			
Power Segment "L"			
P1	3.3V	3.3V power	--
P2	3.3V	3.3V power	--
P3	3.3V	3.3V power	--
P4	GND	Ground signal	--
P5	GND	Ground signal	--
P6	GND	Ground signal	--
P7	5V	5V power	--
P8	5V	5V power	--
P9	5V	5V power	--
P10	GND	Ground signal	--
P11	RES	Reserved	--
P12	GND	Ground signal	--
P13	12V (NC)	Not connected	--
P14	12V (NC)	Not connected	--
P15	12V (NC)	Not connected	--
Power Segment Key			